PRODUCT PREVIEW

80960JD
EMBEDDED 32-BIT MICROPROCESSOR

- Pin/Code Compatible with the 80960JA/JF
- High-Performance Embedded Architecture
  - One Instruction/Clock Execution
  - Core Clock Rate is 2x the Bus Clock
  - Load/Store Programming Model
  - Sixteen 32-Bit Global Registers
  - Sixteen 32-Bit Local Registers (8 sets)
  - Nine Addressing Modes
  - User/Supervisor Protection Model
- Two-Way Set Associative Instruction Cache
  - 4 Kbyte
  - Programmable Cache Locking Mechanism
- Direct Mapped Data Cache
  - 2 Kbyte
  - Write Through Operation
- On-Chip Stack Frame Cache
  - Seven Register Sets Can Be Saved
  - Automatic Allocation on Call/Return
  - 0-7 Frames Reserved for High-Priority Interrupts
- On-Chip Data RAM
  - 1 Kbyte Critical Variable Storage
  - Single-Cycle Access
- High Bandwidth Burst Bus
  - 32-Bit Multiplexed Address/Data
  - Programmable Memory Configuration
  - Selectable 8-, 16-, 32-Bit Bus Widths
  - Supports Unaligned Accesses
  - Big or Little Endian Byte Ordering
- New Instructions
  - Conditional Add, Subtract and Select
  - Processor Management
- High-Speed Interrupt Controller
  - 31 Programmable Priorities
  - Eight Maskable Pins plus NMI
  - Up to 240 Vectors in Expanded Mode
- Two On-Chip Timers
  - Independent 32-Bit Counting
  - Clock Prescaling by 1, 2, 4 or 8
  - Internal Interrupt Sources
- Halt Mode for Low Power
- IEEE 1149.1 (JTAG) Boundary Scan Compatibility
- Packages
  - 132-Lead Pin Grid Array (PGA)
  - 132-Lead Plastic Quad Flat-Pack (PQFP)

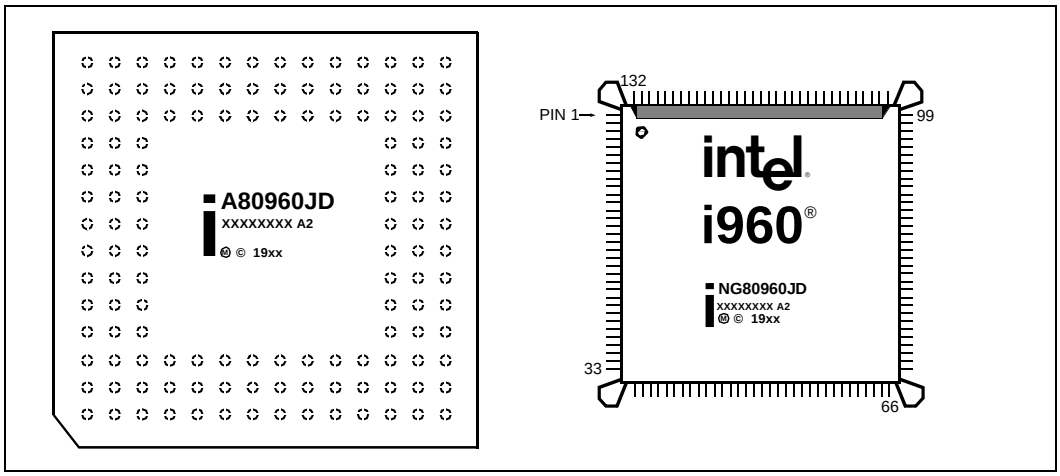

Figure 1. 80960JD Microprocessor

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80960JD
EMBEDDED 32-BIT MICROPROCESSOR

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PRODUCT PREVIEW

1.0 PURPOSE

This document contains advance information for the 80960JD microprocessor, including targeted electrical characteristics and package pinout information. Detailed functional descriptions — other than parametric performance — are published in the *i960® Jx Microprocessor User's Guide* (272483).

The 80960Jx family includes:

- 80960JA — 2 Kbyte instruction cache, 1 Kbyte data cache
- 80960JF — 4 Kbyte instruction cache, 2 Kbyte data cache
- 80960JD — 4 Kbyte instruction cache, 2 Kbyte data cache and clock doubling

2.0 80960JD OVERVIEW

The 80960JD, a new member in the family of embedded i960 processors, provides high performance to cost-sensitive 32-bit embedded applications. The 80960JD is object code compatible with the 80960 Core Architecture and is capable of sustained execution at the rate of one instruction per clock. This processor's features include generous instruction cache, data cache and data RAM. It also boasts a fast interrupt mechanism, dual programmable timer units and new instructions.

The 80960JD's clock doubler operates the processor core at twice the bus clock rate to improve execution performance without increasing the complexity of board designs.

Memory subsystems for cost-sensitive embedded applications often impose substantial wait state penalties. The 80960JD integrates considerable storage resources on-chip to decouple CPU execution from the external bus. The 80960JD includes a 4 Kbyte instruction cache, 2 Kbyte data cache and 1 Kbyte data RAM.

The 80960JD rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

A 32-bit multiplexed burst bus provides a high-speed interface to system memory and I/O. A full complement of control signals simplifies the connection of the 80960JD to external components. The user programs physical and logical memory attributes through memory-mapped control registers (MMRs) — an extension not found on the i960 Kx, Sx or Cx processors. Physical and logical configuration registers enable the processor to operate with all combinations of bus width and data object alignment. The processor supports a homogeneous byte ordering model.

This processor integrates two important peripherals: a timer unit and an interrupt controller. These and other hardware resources are programmed through memory-mapped control registers, an extension to the familiar 80960 architecture.

The timer unit (TU) offers two independent 32-bit timers for use as real-time system clocks and general purpose system timing. These operate in either single-shot or auto-reload mode and can generate interrupts.

The interrupt controller unit (ICU) provides a flexible means for requesting interrupts. The ICU provides full programmability of up to 240 interrupt sources into 31 priority levels. The ICU takes advantage of a cached priority table and optional routine caching to minimize interrupt latency. Clock doubling reduces interrupt latency by 40% compared to the 80960JA/JF. Local registers may be dedicated to high-priority interrupts to further reduce their latency. Acting independently from the core, the ICU compares the priorities of posted interrupts with the current process priority, off-loading this task from the core. The ICU also supports the integrated timer interrupts.

The 80960JD features a Halt mode designed to support applications where low power consumption is critical. The **halt** instruction shuts down instruction execution, resulting in a power savings of up to 90 percent.

The 80960JD's testability features, including ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG), provide a powerful environment for design debug and fault diagnosis.

The *Solutions960*® program features a wide variety of development tools that support the i960 processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

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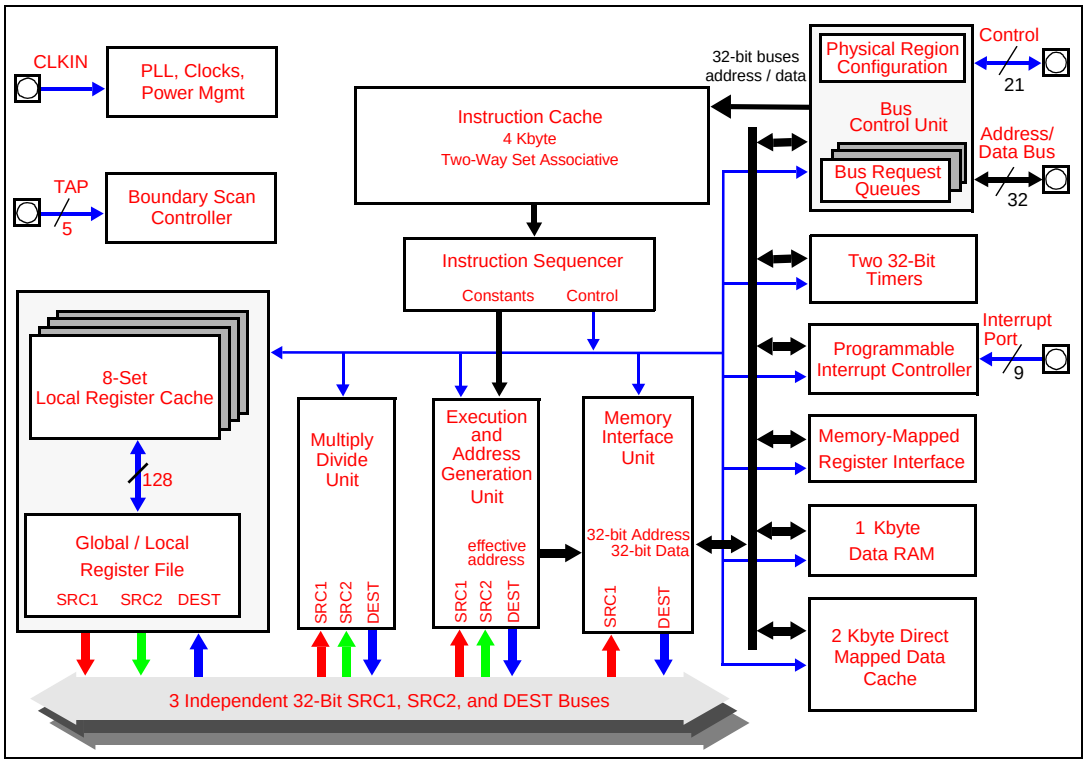


Figure 2. 80960JD Block Diagram

2.1 80960 Processor Core

The 80960Jx family is a new, scalar implementation of the 80960 Core Architecture. Intel designed the processor core to be a very high performance device that is also cost-effective. Factors that contribute to the core's performance include:

- Core operates at twice the bus speed (80960JD only)
- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way set associative, integrated instruction cache
- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated data RAM delivers zero wait state program data

2.2 Burst Bus

A 32-bit high-performance bus controller interfaces the 80960JD to external memory and peripherals. The Bus Control Unit fetches instructions and transfers data at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Users may configure the 80960JD's bus controller to match an application's fundamental memory organization. Physical bus width is register programmed for up to eight regions. Byte ordering and data caching are programmed through a group of logical memory templates and a defaults register.

The Bus Control Unit's features include:

- Multiplexed external bus to minimize pin count
- 32-, 16- and 8-bit bus widths to simplify I/O interfaces
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Support for big or little endian byte ordering to facilitate the porting of existing program code
- Unaligned bus accesses performed transparently
- Three-deep load/store queue to decouple the bus from the core

Upon reset, the 80960JD conducts an internal self test. Then, before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the Initialization Boot Record.

The user may examine the contents of the caches at any time by executing special cache control instructions.

2.3 Timer Unit

The timer unit (TU) contains two independent 32-bit timers which are capable of counting at several clock rates and generating interrupts. Each is programmed by use of the Timer Unit registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960JD's interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected. Clock prescaling is supported.

2.4 Priority Interrupt Controller

A programmable interrupt controller manages up to 240 external sources through an 8-bit external interrupt port. Alternatively, the interrupt inputs may be configured for individual edge- or level-triggered inputs. The Interrupt Unit also accepts interrupts from the two on-chip timer channels and a single Non-Maskable Interrupt ($\overline{\text{NMI}}$) pin. Interrupts are serviced according to their priority levels relative to the current process priority.

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960JD exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space
- Interrupt microcode executes at twice the bus frequency

2.5 Instruction Set Summary

The 80960JD adds several new instructions to the i960 core architecture. The new instructions are:

- Conditional Move
- Conditional Add
- Conditional Subtract
- Byte Swap
- Halt
- Cache Control
- Interrupt Control

Table 1 shows all instructions that are available.

2.6 Faults and Debugging

The 80960JD employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. In software, the 80960JD may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate

trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.7 Low Power Operation

Intel fabricates the 80960JD using an advanced sub-micron manufacturing process. The processor's sub-micron topology provides the circuit density for optimal cache size and high operating speeds while dissipating modest power. The processor also uses dynamic power management to turn off clocks to unused circuits.

Users may program the 80960JD to enter Halt mode for maximum power savings. In Halt mode, the processor core stops completely but the integrated peripherals continue to function, reducing overall power requirements up to 90 percent. Processor execution resumes from internally or externally generated interrupts.

2.8 Test Features

The 80960JD incorporates numerous features which enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960JD provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960JD to electrically "remove" itself from a circuit board. This allows for system-level testing where a remote tester — such as an In-Circuit Emulator (ICE) system — can exercise the processor system.

The provided test logic does not interfere with component or circuit board behavior and ensures that components function correctly, connections between various components are correct, and various components interact correctly on the printed circuit board.

The JTAG Boundary Scan feature is an attractive alternative to conventional "bed-of-nails" testing. It can examine connections which might otherwise be inaccessible to a test system.

2.9 Memory-Mapped Control Registers

The 80960JD, though compliant with i960 series processor core, has the added advantage of memory-mapped, internal control registers not found on the i960 Kx, Sx or Cx processors. These give software the interface to easily read and modify internal control registers.

Each of these registers is accessed as a memory-mapped, 32-bit register. Access is accomplished through regular memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.10 Data Types and Memory Addressing Modes

As with all i960 family processors, the 80960JD instruction set supports several different data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960JD provides a full set of addressing modes for C and assembly:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement
- IP with displacement

Table 1. 80960JD Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load	Add	And	Set Bit
Store	Subtract	Not And	Clear Bit
Move	Multiply	And Not	Not Bit
*Conditional Select	Divide	Or	Alter Bit
Load Address	Remainder	Exclusive Or	Scan For Bit
	Modulo	Not Or	Span Over Bit
	Shift	Or Not	Extract
	Extended Shift	Nor	Modify
	Extended Multiply	Exclusive Nor	Scan Byte for Equal
	Extended Divide	Not	*Byte Swap
	Add with Carry	Nand	
	Subtract with Carry		
	*Conditional Add		
	*Conditional Subtract		
	Rotate		
Comparison	**Branch**	**Call/Return**	**Fault**
Compare	Unconditional Branch	Call	Conditional Fault
Conditional Compare	Conditional Branch	Call Extended	Synchronize Faults
Compare and Increment	Compare and Branch	Call System	
Compare and Decrement		Return	
Test Condition Code		Branch and Link	
Check Bit			
Debug	**Processor Management**	**Atomic**	
Modify Trace Controls	Flush Local Registers	Atomic Add	
Mark	Modify Arithmetic Controls	Atomic Modify	
Force Mark	Modify Process Controls		
	*Halt		
	System Control		
	*Cache Control		
	*Interrupt Control		

* Denotes new 80960Jx instructions unavailable on 80960CA/CF, 80960KA/KB and 80960SA/SB implementations.

3.0 PACKAGE INFORMATION

The 80960JD will be offered in several speed and package grades. The following 132-pin Pin Grid Array (PGA) device will be specified for operation at V_{cc}=5.0V±5% over a case temperature range of 0° to 85°C:

- A80960JD-50 (50 MHz core, 25 MHz bus)

The following 132-pin Pin Grid Array (PGA) devices will be specified for operation at V_{cc}=5.0V±5% over a case temperature range of 0° to 100°C:

- A80960JD-40 (40 MHz core, 20 MHz bus)
- A80960JD-33 (33.33 MHz core, 16.67 MHz bus)

The following 132-pin Plastic Quad Flatpack (PQFP) devices will be specified for operation at V_{cc}=5.0V±5% over a case temperature range of 0° to 100°C:

- NG80960JD-40 (40 MHz core, 20 MHz bus)
- NG80960JD-33 (33.33 MHz core, 16.67 MHz bus)

For complete package specifications and information, refer to Intel's *Packaging Handbook* (Order No. 240800).

3.1 Pin Descriptions

This section describes the pins for the 80960JD in the 132-pin ceramic Pin Grid Array (PGA) package and 132-lead Plastic Quad Flatpack Package (PQFP).

Section 3.1.1, Functional Pin Definitions describes pin function; **Section 3.1.2, 80960JD 132-Lead PGA Pinout** and **Section 3.1.3, 80960JD PQFP Pinout** define the signal and pin locations for the supported package types.

3.1.1 Functional Pin Definitions

Table 2 presents the legend for interpreting the pin descriptions which follow. Pins associated with the bus interface are described in Table 3. Pins associated with basic control and test functions are described in Table 4. Pins associated with the Interrupt Unit are described in Table 5.

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input pin only.
O	Output pin only.
I/O	Pin can be either an input or output.
–	Pin must be connected as described.
S	Synchronous. Inputs must meet setup and hold times relative to CLKIN for proper operation. S(E) Edge sensitive input S(L) Level sensitive input
A (...)	Asynchronous. Inputs may be asynchronous relative to CLKIN. A(E) Edge sensitive input A(L) Level sensitive input
R (...)	While the processor's $\overline{\text{RESET}}$ pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Q) is a valid output R(X) is driven to unknown state R(H) is pulled up to V_{CC}
H (...)	While the processor is in the hold state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Q) Maintains previous state or continues to be a valid output H(Z) Floats
P (...)	While the processor is halted, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Q) Maintains previous state or continues to be a valid output

Table 3. Pin Description — External Bus Signals (Sheet 1 of 3)

NAME	TYPE	DESCRIPTION
AD31:0	**I/O** S(L) R(X) H(Z) P(Q)	**ADDRESS / DATA BUS** carries 32-bit physical addresses and 8-, 16- or 32-bit data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising AD31:24, AD23:16, AD15:8 and AD7:0. During write operations, unused pins are driven to determinate values. SIZE, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction. AD1 AD0 Bus Transfers 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers When the processor enters Halt mode, if the previous bus operation was a: • write — AD31:2 are driven with the last data value on the AD bus. • read — AD31:4 are driven with the last address value on the AD bus; AD3:2 are driven with the value of A3:2 from the last data cycle. Typically, AD1:0 reflect the SIZE information of the last bus transaction (either instruction fetch or load/store) that was executed before entering Halt mode.
ALE	**O** R(0) H(Z) P(0)	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).
$\overline{\text{ALE}}$	**O** R(1) H(Z) P(1)	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. $\overline{\text{ALE}}$ is the inverted version of ALE. This signal gives the 80960JD a high degree of compatibility with existing 80960Kx systems.
$\overline{\text{ADS}}$	**O** R(1) H(Z) P(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. The processor asserts $\overline{\text{ADS}}$ for the entire T_a cycle. External bus control logic typically samples $\overline{\text{ADS}}$ at the end of the cycle.
A3:2	**O** R(X) H(Z) P(Q)	**ADDRESS3:2** comprise a partial demultiplexed address bus. *32-bit memory accesses:* the processor asserts address bits A3:2 during T_a. The partial word address increments with each assertion of $\overline{\text{RDYRCV}}$ during a burst. *16-bit memory accesses:* the processor asserts address bits A3:1 during T_a with A1 driven on the $\overline{\text{BE1}}$ pin. The partial short word address increments with each assertion of $\overline{\text{RDYRCV}}$ during a burst. *8-bit memory accesses:* the processor asserts address bits A3:0 during T_a, with A1:0 driven on $\overline{\text{BE1:0}}$. The partial byte address increments with each assertion of $\overline{\text{RDYRCV}}$ during a burst.

Table 3. Pin Description — External Bus Signals (Sheet 2 of 3)

NAME	TYPE	DESCRIPTION
$\overline{BE3:0}$	**O** R(1) H(Z) P(1)	**BYTE ENABLES** select which of up to four data bytes on the bus participate in the current bus access. Byte enable encoding is dependent on the bus width of the memory region accessed: *32-bit bus:* $\overline{BE3}$ enables data on AD31:24 $\overline{BE2}$ enables data on AD23:16 $\overline{BE1}$ enables data on AD15:8 $\overline{BE0}$ enables data on AD7:0 *16-bit bus:* $\overline{BE3}$ becomes Byte High Enable (enables data on AD15:8) $\overline{BE2}$ is not used (state is high) $\overline{BE1}$ becomes Address Bit 1 (A1) $\overline{BE0}$ becomes Byte Low Enable (enables data on AD7:0) *8-bit bus:* $\overline{BE3}$ is not used (state is high) $\overline{BE2}$ is not used (state is high) $\overline{BE1}$ becomes Address Bit 1 (A1) $\overline{BE0}$ becomes Address Bit 0 (A0) The processor asserts byte enables, byte high enable and byte low enable during T_a. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during a burst. They remain active through the last T_d cycle. For accesses to 8- and 16-bit memory, the processor asserts the address bits in conjunction with A3:2 described above.
WIDTH/ HLTD1:0	**O** R(0) H(Z) P(1)	**WIDTH/HALTED** signals denote the physical memory attributes for a bus transaction: WIDTH/HLTD1 — WIDTH/HLTD0 0 — 0 — 8 Bits Wide 0 — 1 — 16 Bits Wide 1 — 0 — 32 Bits Wide 1 — 1 — Processor Halted The processor floats the WIDTH/HLTD pins whenever it relinquishes the bus in response to a HOLD request, regardless of prior operating state.
D/$\overline{C}$	**O** R(X) H(Z) P(Q)	**DATA/CODE** indicates that a bus access is a data access (1) or an instruction access (0). D/$\overline{C}$ has the same timing as W/$\overline{R}$.
W/$\overline{R}$	**O** R(0) H(Z) P(Q)	**WRITE/READ** specifies, during a T_a cycle, whether the operation is a write (1) or read (0). It is latched on-chip and remains valid during T_d cycles.
DT/$\overline{R}$	**O** R(0) H(Z) P(Q)	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the address/data bus. It is low during T_a and T_w/T_d cycles for a read; it is high during T_a and T_w/T_d cycles for a write. DT/$\overline{R}$ never changes state when $\overline{DEN}$ is asserted.

Table 3. Pin Description — External Bus Signals (Sheet 3 of 3)

NAME	TYPE	DESCRIPTION
$\overline{\text{DEN}}$	**O** R(1) H(Z) P(1)	**DATA ENABLE** indicates data transfer cycles during a bus access. $\overline{\text{DEN}}$ is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. $\overline{\text{DEN}}$ is used with DT/$\overline{\text{R}}$ to provide control for data transceivers connected to the data bus.
$\overline{\text{BLAST}}$	**O** R(1) H(Z) P(1)	**BURST LAST** indicates the last transfer in a bus access. $\overline{\text{BLAST}}$ is asserted in the last data transfer of burst and non-burst accesses. $\overline{\text{BLAST}}$ remains active as long as wait states are inserted via the $\overline{\text{RDYRCV}}$ pin. $\overline{\text{BLAST}}$ becomes inactive after the final data transfer in a bus cycle.
$\overline{\text{RDYRCV}}$	**I** S(L)	**READY/RECOVER** indicates that data on AD lines can be sampled or removed. If $\overline{\text{RDYRCV}}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w). The $\overline{\text{RDYRCV}}$ pin has an alternate function during the recovery (T_r) state. The processor continues to insert additional recovery states until it samples the pin HIGH. This function allows slow external devices longer to float their buffers before the processor begins to drive address again.
$\overline{\text{LOCK}}$/ $\overline{\text{ONCE}}$	**I/O** S(L) R(H) H(Z) P(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. The $\overline{\text{LOCK}}$ output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant HOLDA while it is asserting $\overline{\text{LOCK}}$. This prevents external agents from accessing memory involved in semaphore operations. **ONCE MODE:** The processor samples the $\overline{\text{ONCE}}$ input during reset. If it is asserted LOW at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins. The pin has a weak internal pullup which is active during reset to ensure normal operation if the pin is left unconnected.
HOLD	**I** S(L)	**HOLD**: A request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it asserts HOLDA, floats the address/data and control lines and enters the T_h state. When HOLD is deasserted, the processor deasserts HOLDA and enters either the T_i or T_a state, resuming control of the address/data and control lines.
HOLDA	**O** R(Q) H(1) P(Q)	**HOLD ACKNOWLEDGE** indicates to an external bus master that the processor has relinquished control of the bus. The processor can grant HOLD requests and enter the T_h state during reset and while halted as well as during regular operation.
BSTAT	**O** R(0) H(Q) P(0)	**BUS STATUS** indicates that the processor may soon stall unless it has sufficient access to the bus; see *i960® Jx Microprocessor User's Guide* (272483). Arbitration logic can examine this signal to determine when an external bus master should acquire/relinquish the bus.

Table 4. Pin Description — Processor Control Signals, Test Signals and Power (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLKIN	**I**	**CLOCK INPUT** provides the processor's fundamental time base; both the processor core and the external bus run at the CLKIN rate. All input and output timings are specified relative to a rising CLKIN edge.
$\overline{\text{RESET}}$	**I** A(L)	**RESET** initializes the processor and clears its internal logic. During reset, the processor places the address/data bus and control output pins in their idle (inactive) states. During reset, the input pins are ignored with the exception of $\overline{\text{LOCK}}$/$\overline{\text{ONCE}}$, STEST and HOLD. The $\overline{\text{RESET}}$ pin has an internal synchronizer. To ensure predictable processor initialization during power up, $\overline{\text{RESET}}$ must be asserted a minimum of 10,000 CLKIN cycles with V_{CC} and CLKIN stable. On a warm reset, $\overline{\text{RESET}}$ should be asserted for a minimum of 15 cycles.
STEST	**I** S(L)	**SELF TEST** enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of reset. If STEST is asserted, the processor performs its internal self-test and the external bus confidence test. If STEST is deasserted, the processor performs only the external bus confidence test.
$\overline{\text{FAIL}}$	**O** R(0) H(Q) P(1)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. $\overline{\text{FAIL}}$ is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: • If self-test passes, the processor deasserts $\overline{\text{FAIL}}$ and begins operation from user code. • If self-test fails, the processor asserts $\overline{\text{FAIL}}$ and then stops executing.
TCK	**I**	**TEST CLOCK** is a CPU input which provides the clocking function for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the processor on the rising edge; data is clocked out of the processor on the falling edge.
TDI	**I** S(L)	**TEST DATA INPUT** is the serial input pin for JTAG. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port.
TDO	**O** R(Q) HQ) P(Q)	**TEST DATA OUTPUT** is the serial output pin for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats. TDO does not float during ONCE mode.
$\overline{\text{TRST}}$	**I** A(L)	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan testing (JTAG). When using the Boundary Scan feature, connect a pulldown resistor between this pin and V_{SS}. If you are not using the TAP, this pin must be connected to V_{SS}; however, no resistor is required.

Table 4. Pin Description — Processor Control Signals, Test Signals and Power (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
TMS	**I** S(L)	**TEST MODE SELECT** is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing.
V_{CC}	–	**POWER** leads intended for external connection to a V_{CC} board plane.
V_{CCPLL}	–	**PLL POWER** is a separate V_{CC} supply lead for the phase lock loop clock generator. It is intended for external connection to the V_{CC} board plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
V_{SS}	–	**GROUND** leads intended for external connection to a V_{SS} board plane.
N.C.	–	**NO CONNECT** leads. Do not make any system connections to these leads.

Table 5. Pin Description — Interrupt Unit Signals

NAME	TYPE	DESCRIPTION
$\overline{\text{XINT7:0}}$	**I** A(E/L)	**EXTERNAL INTERRUPT** pins are used to request interrupt service. The $\overline{\text{XINT7:0}}$ pins can be configured in three modes: **Dedicated Mode**: Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be level (low) or edge (falling) sensitive. **Expanded Mode**: All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode. **Mixed Mode**: The $\overline{\text{XINT7:5}}$ pins act as dedicated sources and the $\overline{\text{XINT4:0}}$ pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to 010_2 internally. Unused external interrupt pins should be connected to V_{CC}.
$\overline{\text{NMI}}$	**I** A(E)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. $\overline{\text{NMI}}$ is the highest priority interrupt source and is falling edge-triggered. If $\overline{\text{NMI}}$ is unused, it should be connected to V_{CC}.

3.1.2 80960JD 132-Lead PGA Pinout

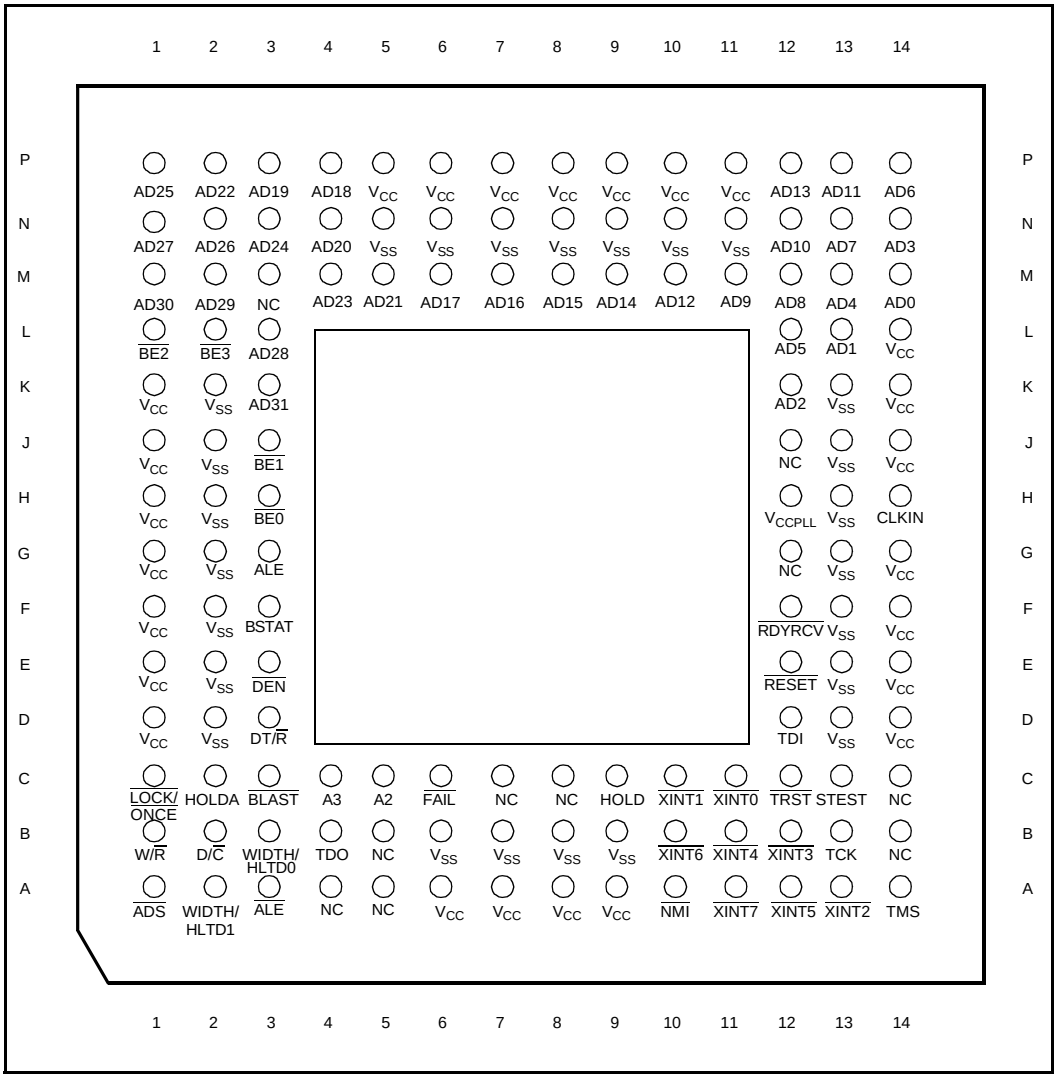


Figure 3. 132-Lead Pin Grid Array Bottom View - Pins Facing Up

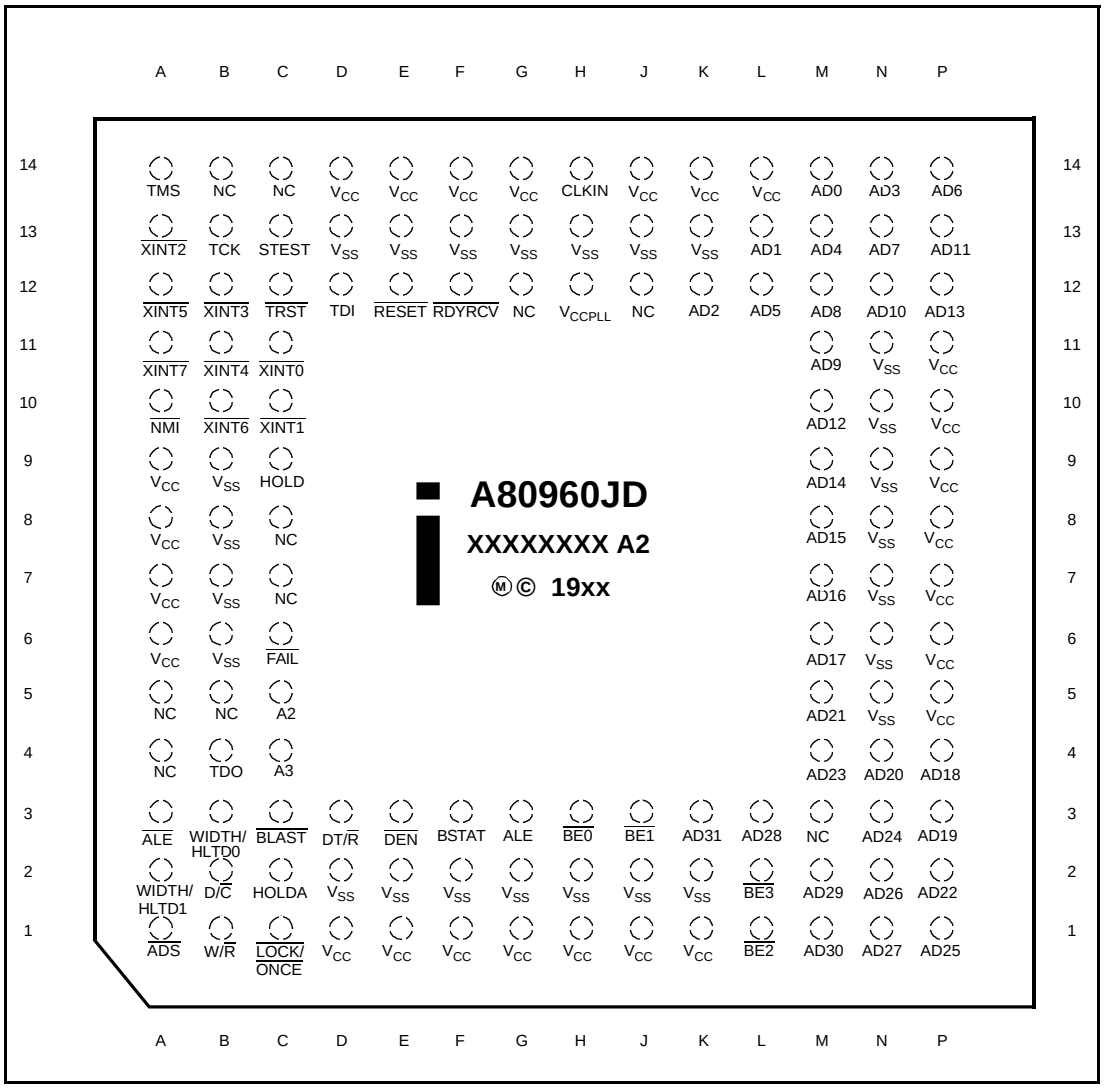


Figure 4. 132-Lead Pin Grid Array Top View - Pins Facing Down

Table 6. 132-Lead PGA Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	C5	AD31	K3	TDI	D12	V_{SS}	B9
A3	C4	$\overline{ADS}$	A1	TDO	B4	V_{SS}	D2
AD0	M14	ALE	G3	TMS	A14	V_{SS}	D13
AD1	L13	$\overline{ALE}$	A3	$\overline{TRST}$	C12	V_{SS}	E2
AD2	K12	$\overline{BE0}$	H3	V_{CC}	A6	V_{SS}	E13
AD3	N14	$\overline{BE1}$	J3	V_{CC}	A7	V_{SS}	F2
AD4	M13	$\overline{BE2}$	L1	V_{CC}	A8	V_{SS}	F13
AD5	L12	$\overline{BE3}$	L2	V_{CC}	A9	V_{SS}	G2
AD6	P14	$\overline{BLAST}$	C3	V_{CC}	D1	V_{SS}	G13
AD7	N13	BSTAT	F3	V_{CC}	D14	V_{SS}	H2
AD8	M12	CLKIN	H14	V_{CC}	E1	V_{SS}	H13
AD9	M11	D/$\overline{C}$	B2	V_{CC}	E14	V_{SS}	J2
AD10	N12	$\overline{DEN}$	E3	V_{CC}	F1	V_{SS}	J13
AD11	P13	DT/$\overline{R}$	D3	V_{CC}	F14	V_{SS}	K2
AD12	M10	$\overline{FAIL}$	C6	V_{CC}	G1	V_{SS}	K13
AD13	P12	HOLD	C9	V_{CC}	G14	V_{SS}	N5
AD14	M9	HOLDA	C2	V_{CC}	H1	V_{SS}	N6
AD15	M8	$\overline{LOCK/ONCE}$	C1	V_{CC}	J1	V_{SS}	N7
AD16	M7	NC	A4	V_{CC}	J14	V_{SS}	N8
AD17	M6	NC	A5	V_{CC}	K1	V_{SS}	N9
AD18	P4	NC	B5	V_{CC}	K14	V_{SS}	N10
AD19	P3	NC	B14	V_{CC}	L14	V_{SS}	N11
AD20	N4	NC	C7	V_{CC}	P5	W/$\overline{R}$	B1
AD21	M5	NC	C8	V_{CC}	P6	WIDTH/HLTD0	B3
AD22	P2	NC	C14	V_{CC}	P7	WIDTH/HLTD1	A2
AD23	M4	NC	G12	V_{CC}	P8	$\overline{XINT0}$	C11
AD24	N3	NC	J12	V_{CC}	P9	$\overline{XINT1}$	C10
AD25	P1	NC	M3	V_{CC}	P10	$\overline{XINT2}$	A13
AD26	N2	$\overline{NMI}$	A10	V_{CC}	P11	$\overline{XINT3}$	B12
AD27	N1	$\overline{RDYRCV}$	F12	V_{CCPLL}	H12	$\overline{XINT4}$	B11
AD28	L3	$\overline{RESET}$	E12	V_{SS}	B6	$\overline{XINT5}$	A12
AD29	M2	STEST	C13	V_{SS}	B7	$\overline{XINT6}$	B10
AD30	M1	TCK	B13	V_{SS}	B8	$\overline{XINT7}$	A11

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 7. 132-Lead PGA Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	$\overline{ADS}$	C6	$\overline{FAIL}$	H1	V_{CC}	M10	AD12
A2	WIDTH/HLTD1	C7	NC	H2	V_{SS}	M11	AD9
A3	$\overline{ALE}$	C8	NC	H3	$\overline{BE0}$	M12	AD8
A4	NC	C9	HOLD	H12	V_{CCPLL}	M13	AD4
A5	NC	C10	$\overline{XINT1}$	H13	V_{SS}	M14	AD0
A6	V_{CC}	C11	$\overline{XINT0}$	H14	CLKIN	N1	AD27
A7	V_{CC}	C12	$\overline{TRST}$	J1	V_{CC}	N2	AD26
A8	V_{CC}	C13	STEST	J2	V_{SS}	N3	AD24
A9	V_{CC}	C14	NC	J3	$\overline{BE1}$	N4	AD20
A10	$\overline{NMI}$	D1	V_{CC}	J12	NC	N5	V_{SS}
A11	$\overline{XINT7}$	D2	V_{SS}	J13	V_{SS}	N6	V_{SS}
A12	$\overline{XINT5}$	D3	DT/$\overline{R}$	J14	V_{CC}	N7	V_{SS}
A13	$\overline{XINT2}$	D12	TDI	K1	V_{CC}	N8	V_{SS}
A14	TMS	D13	V_{SS}	K2	V_{SS}	N9	V_{SS}
B1	W/$\overline{R}$	D14	V_{CC}	K3	AD31	N10	V_{SS}
B2	D/$\overline{C}$	E1	V_{CC}	K12	AD2	N11	V_{SS}
B3	WIDTH/HLTD0	E2	V_{SS}	K13	V_{SS}	N12	AD10
B4	TDO	E3	$\overline{DEN}$	K14	V_{CC}	N13	AD7
B5	NC	E12	$\overline{RESET}$	L1	$\overline{BE2}$	N14	AD3
B6	V_{SS}	E13	V_{SS}	L2	$\overline{BE3}$	P1	AD25
B7	V_{SS}	E14	V_{CC}	L3	AD28	P2	AD22
B8	V_{SS}	F1	V_{CC}	L12	AD5	P3	AD19
B9	V_{SS}	F2	V_{SS}	L13	AD1	P4	AD18
B10	$\overline{XINT6}$	F3	BSTAT	L14	V_{CC}	P5	V_{CC}
B11	$\overline{XINT4}$	F12	$\overline{RDYRCV}$	M1	AD30	P6	V_{CC}
B12	$\overline{XINT3}$	F13	V_{SS}	M2	AD29	P7	V_{CC}
B13	TCK	F14	V_{CC}	M3	NC	P8	V_{CC}
B14	NC	G1	V_{CC}	M4	AD23	P9	V_{CC}
C1	$\overline{LOCK}$/$\overline{ONCE}$	G2	V_{SS}	M5	AD21	P10	V_{CC}
C2	HOLDA	G3	ALE	M6	AD17	P11	V_{CC}
C3	$\overline{BLAST}$	G12	NC	M7	AD16	P12	AD13
C4	A3	G13	V_{SS}	M8	AD15	P13	AD11
C5	A2	G14	V_{CC}	M9	AD14	P14	AD6

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.1.3 80960JD PQFP Pinout

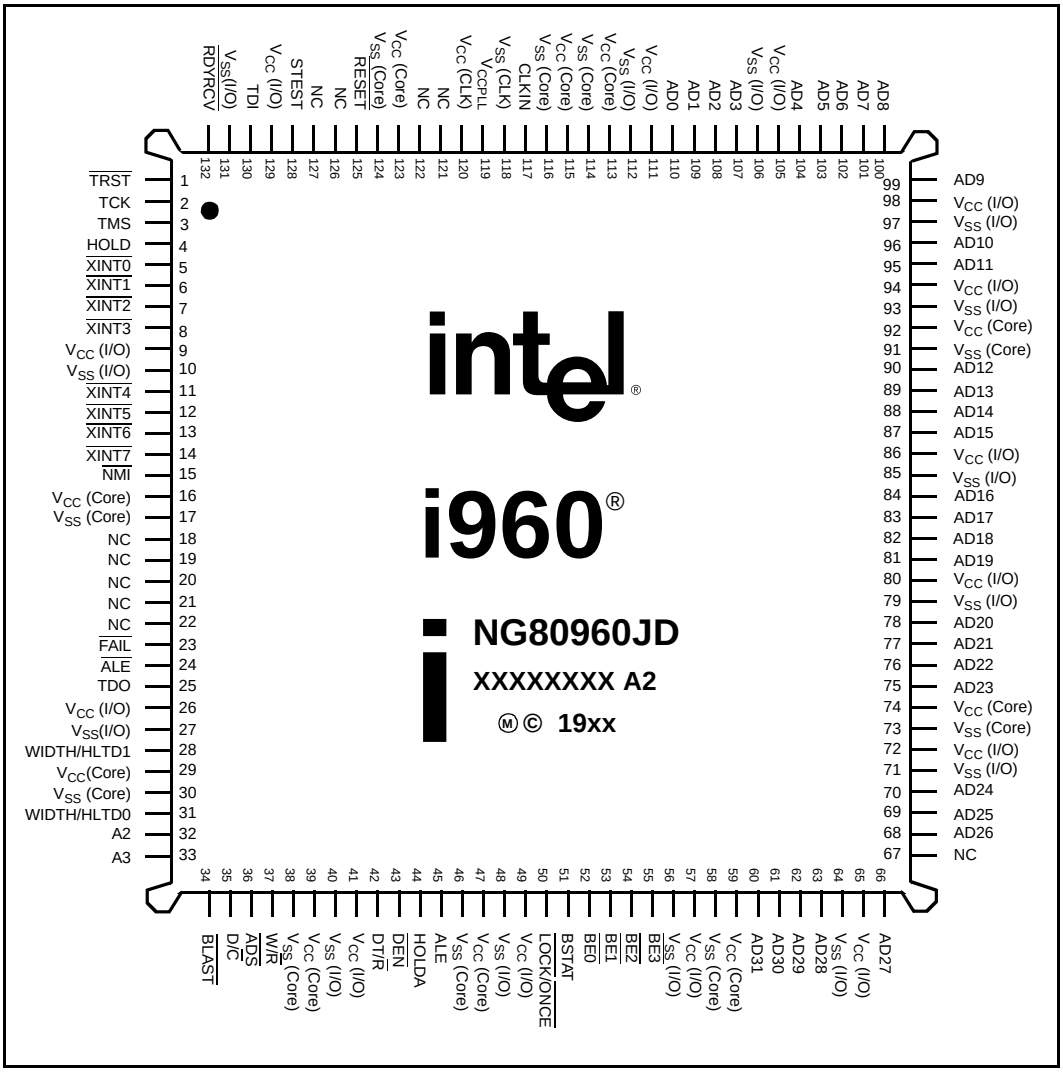


Figure 5. 132-Lead PQFP - Top View

Table 8. 132-Lead PQFP Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD31	60	$\overline{ALE}$	24	V_{CC} (Core)	47	V_{SS} (I/O)	10
AD30	61	$\overline{ADS}$	36	V_{CC} (Core)	59	V_{SS} (I/O)	27
AD29	62	A3	33	V_{CC} (Core)	74	V_{SS} (I/O)	40
AD28	63	A2	32	V_{CC} (Core)	92	V_{SS} (I/O)	48
AD27	66	$\overline{BE3}$	55	V_{CC} (Core)	113	V_{SS} (I/O)	56
AD26	68	$\overline{BE2}$	54	V_{CC} (Core)	115	V_{SS} (I/O)	64
AD25	69	$\overline{BE1}$	53	V_{CC} (Core)	123	V_{SS} (I/O)	71
AD24	70	$\overline{BE0}$	52	V_{CC} (I/O)	9	V_{SS} (I/O)	79
AD23	75	WIDTH/HLTD1	28	V_{CC} (I/O)	26	V_{SS} (I/O)	85
AD22	76	WIDTH/HLTD0	31	V_{CC} (I/O)	41	V_{SS} (I/O)	93
AD21	77	D/$\overline{C}$	35	V_{CC} (I/O)	49	V_{SS} (I/O)	97
AD20	78	W/$\overline{R}$	37	V_{CC} (I/O)	57	V_{SS} (I/O)	106
AD19	81	DT/$\overline{R}$	42	V_{CC} (I/O)	65	V_{SS} (I/O)	112
AD18	82	$\overline{DEN}$	43	V_{CC} (I/O)	72	V_{SS} (I/O)	131
AD17	83	$\overline{BLAST}$	34	V_{CC} (I/O)	80	NC	18
AD16	84	$\overline{RDYRCV}$	132	V_{CC} (I/O)	86	NC	19
AD15	87	$\overline{LOCK}$/$\overline{ONCE}$	50	V_{CC} (I/O)	94	NC	20
AD14	88	HOLD	4	V_{CC} (I/O)	98	NC	21
AD13	89	HOLDA	44	V_{CC} (I/O)	105	NC	22
AD12	90	BSTAT	51	V_{CC} (I/O)	111	NC	67
AD11	95	CLKIN	117	V_{CC} (I/O)	129	NC	121
AD10	96	$\overline{RESET}$	125	V_{CCPLL}	119	NC	122
AD9	99	STEST	128	V_{SS} (CLK)	118	NC	126
AD8	100	$\overline{FAIL}$	23	V_{SS} (Core)	17	NC	127
AD7	101	TCK	2	V_{SS} (Core)	30	$\overline{XINT7}$	14
AD6	102	TDI	130	V_{SS} (Core)	38	$\overline{XINT6}$	13
AD5	103	TDO	25	V_{SS} (Core)	46	$\overline{XINT5}$	12
AD4	104	$\overline{TRST}$	1	V_{SS} (Core)	58	$\overline{XINT4}$	11
AD3	107	TMS	3	V_{SS} (Core)	73	$\overline{XINT3}$	8
AD2	108	V_{CC} (CLK)	120	V_{SS} (Core)	91	$\overline{XINT2}$	7
AD1	109	V_{CC} (Core)	16	V_{SS} (Core)	114	$\overline{XINT1}$	6
AD0	110	V_{CC} (Core)	29	V_{SS} (Core)	116	$\overline{XINT0}$	5
ALE	45	V_{CC} (Core)	39	V_{SS} (Core)	124	$\overline{NMI}$	15

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 9. 132-Lead PQFP Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	$\overline{TRST}$	34	$\overline{BLAST}$	67	NC	100	AD8
2	TCK	35	D/$\overline{C}$	68	AD26	101	AD7
3	TMS	36	$\overline{ADS}$	69	AD25	102	AD6
4	HOLD	37	W/$\overline{R}$	70	AD24	103	AD5
5	$\overline{XINT0}$	38	V_{SS} (Core)	71	V_{SS} (I/O)	104	AD4
6	$\overline{XINT1}$	39	V_{CC} (Core)	72	V_{CC} (I/O)	105	V_{CC} (I/O)
7	$\overline{XINT2}$	40	V_{SS} (I/O)	73	V_{SS} (Core)	106	V_{SS} (I/O)
8	$\overline{XINT3}$	41	V_{CC} (I/O)	74	V_{CC} (Core)	107	AD3
9	V_{CC} (I/O)	42	DT/$\overline{R}$	75	AD23	108	AD2
10	V_{SS} (I/O)	43	$\overline{DEN}$	76	AD22	109	AD1
11	$\overline{XINT4}$	44	HOLDA	77	AD21	110	AD0
12	$\overline{XINT5}$	45	ALE	78	AD20	111	V_{CC} (I/O)
13	$\overline{XINT6}$	46	V_{SS} (Core)	79	V_{SS} (I/O)	112	V_{SS} (I/O)
14	$\overline{XINT7}$	47	V_{CC} (Core)	80	V_{CC} (I/O)	113	V_{CC} (Core)
15	$\overline{NMI}$	48	V_{SS} (I/O)	81	AD19	114	V_{SS} (Core)
16	V_{CC} (Core)	49	V_{CC} (I/O)	82	AD18	115	V_{CC} (Core)
17	V_{SS} (Core)	50	$\overline{LOCK}$/$\overline{ONCE}$	83	AD17	116	V_{SS} (Core)
18	NC	51	BSTAT	84	AD16	117	CLKIN
19	NC	52	$\overline{BE0}$	85	V_{SS} (I/O)	118	V_{SS} (CLK)
20	NC	53	$\overline{BE1}$	86	V_{CC} (I/O)	119	V_{CCPLL}
21	NC	54	$\overline{BE2}$	87	AD15	120	$V_{CC\ (CLK)}$
22	NC	55	$\overline{BE3}$	88	AD14	121	NC
23	$\overline{FAIL}$	56	V_{SS} (I/O)	89	AD13	122	NC
24	$\overline{ALE}$	57	V_{CC} (I/O)	90	AD12	123	V_{CC} (Core)
25	TDO	58	V_{SS} (Core)	91	V_{SS} (Core)	124	V_{SS} (Core)
26	V_{CC} (I/O)	59	V_{CC} (Core)	92	V_{CC} (Core)	125	$\overline{RESET}$
27	V_{SS} (I/O)	60	AD31	93	V_{SS} (I/O)	126	NC
28	WIDTH/HLTD1	61	AD30	94	V_{CC} (I/O)	127	NC
29	V_{CC} (Core)	62	AD29	95	AD11	128	STEST
30	V_{SS} (Core)	63	AD28	96	AD10	129	V_{CC} (I/O)
31	WIDTH/HLTD0	64	V_{SS} (I/O)	97	V_{SS} (I/O)	130	TDI
32	A2	65	V_{CC} (I/O)	98	V_{CC} (I/O)	131	V_{SS} (I/O)
33	A3	66	AD27	99	AD9	132	$\overline{RDYRCV}$

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.2 Package Thermal Specifications

The 80960JD is specified for operation when T_C (case temperature) is within the range of 0°C to 85°C for the(PGA) 80960JD-50, or 0°C to 100°C for the (PQFP and PGA) 80960JD-40 and 80960JD-33. Case temperature may be measured in any environment to determine whether the 80960JD is within specified operating range. The case temperature should be measured at the center of the top surface, opposite the pins.

θ_{CA} is the thermal resistance from case to ambient. Use the following equation to calculate T_A, the maximum ambient temperature to conform to a particular case temperature:

$T_A = T_C - P (\theta_{CA})$

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$T_J = T_C + P (\theta_{JC})$

Similarly, if T_A is known, the corresponding case temperature, T_C, can be calculated as follows:

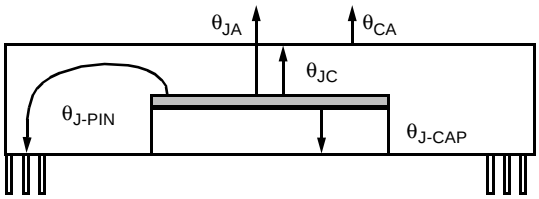
$T_C = T_A + P (\theta_{CA})$

Compute P by multiplying I_{CC} from Table 13 and V_{CC}. Values for θ_{JC} and θ_{CA} are given in Table 10 for the PGA package and Table 11 for the PQFP package. For high speed operation, the processor's θ_{JA} may be significantly reduced by adding a heatsink and/or by increasing airflow.

Figure 6 shows the maximum ambient temperature (T_A) permitted without exceeding T_C for the 80960JD-50 in a PGA package. Figure 7 illustrates this for the 80960JD-40 in PGA and PQFP packages. The curves are based on minimum I_{CC} (hot) and maximum V_{CC} of +5.25 V, with a T_{CASE} of +85°C for the 80960JD-50, or a T_{CASE} of +100°C for the 80960JD-40.

Table 10. 132-Lead PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	**Airflow — ft./min (m/sec)**					
	0 (0)	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**	**1000 (5.08)**
θ_{JC} (Junction-to-Case)	3	3	3	3	3	3
θ_{CA} (Case-to-Ambient) (No Heatsink)	18	15	12	11	11	11
θ_{CA} (Case-to-Ambient) (Omnidirectional Heatsink)	15	12	9	8	8	8
θ_{CA} (Case-to-Ambient) (Unidirectional Heatsink)	14	11	8	7	7	7

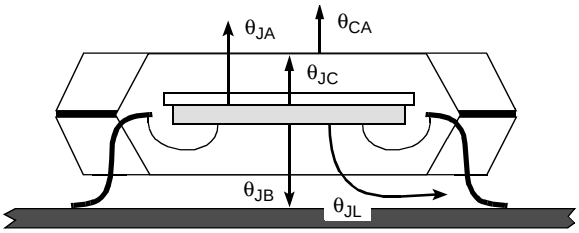


NOTES:

1. This table applies to a PGA device plugged into a socket or soldered directly into a board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{J\text{-}CAP}$ = 4°C/W (approx.)
4. $\theta_{J\text{-}PIN}$ = 4°C/W (inner pins) (approx.)
5. $\theta_{J\text{-}PIN}$ = 8°C/W (outer pins) (approx.)

Table 11. 132-Lead PQFP Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	**Airflow — ft./min (m/sec)**						
	0 (0)	**50 (0.25)**	**100 (0.50)**	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**
θ_{JC} (Junction-to-Case)	6	7	7	7	7	7	7
θ_{CA} (Case-to-Ambient -No Heatsink)	23	20	18	14	10	9	8



NOTES:
1. This table applies to a PQFP device soldered directly into board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. θ_{JL} = 18°C/W (approx.)
4. θ_{JB} = 18°C/W (approx.)

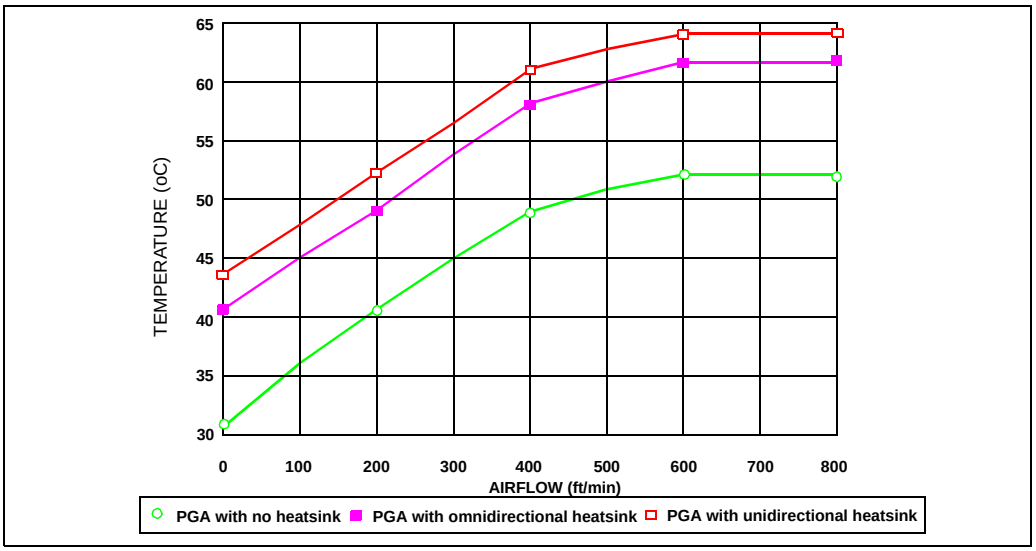


Figure 6. 50 MHz Maximum Allowable Ambient Temperature

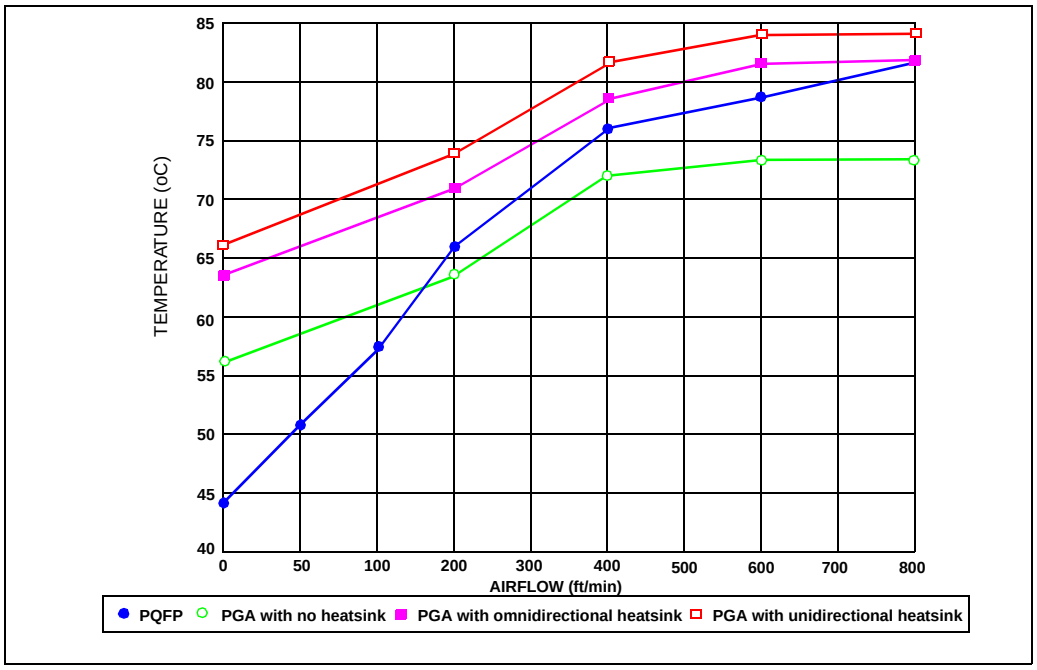


Figure 7. 40 MHz Maximum Allowable Ambient Temperature

3.3 Thermal Management Accessories

The following is a list of suggested sources for 80960JD accessories. This is neither an endorsement or a warranty of the performance of any of the listed products and/or companies.

Heatsinks

1. Thermalloy, Inc.
   2021 West Valley View Lane
   Dallas, TX 75234-8993
   (214) 243-4321 FAX: (214) 241-4656
2. Wakefield Engineering
   60 Audubon Road
   Wakefield, MA 01880
   (617) 245-5900
3. Aavid Engineering
   One Kool Path
   Laconia, NH 03247-0400
   (603) 528-3400

Conformal Thermal Materials

1. 3M Co.
   3M Center, Bldg. 223-65-04
   St. Paul, MN 55144-1000
   (800) 364-3577

4.0 ELECTRICAL SPECIFICATIONS

NOTICE: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available.

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Case Temperature Under Bias	–65°C to +110°C
Supply Voltage wrt. V_{SS}	–0.5V to + 6.5V
Voltage on Other Pins wrt. V_{SS}	–0.5V to V_{CC} + 0.5V

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Operating Conditions

Table 12. Targeted 80960JD Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage				
	80960JD-50	4.75	5.25	V	
	80960JD-40	4.75	5.25		
	80960JD-33	4.75	5.25		
f_{CLKIN}	Input Clock Frequency				
	80960JD-50	8	25	MHz	
	80960JD-40	8	20		
	80960JD-33	8	16.67		
T_C	Operating Case Temperature				
	A80960JD-50 (132 PGA)	0	85	°C	
	A80960JD-40 (132 PGA)	0	100		
	NG80960JD-40 (132 PQFP)	0	100		
	A80960JD-33 (132 PGA)	0	100		
	NG80960JD-33 (132 PQFP)	0	100		

4.3 Connection Recommendations

For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960JD power and ground pins. On the circuit board, every V_{CC} pin should connect to a power plane and every V_{SS} pin should connect to a ground plane. Place liberal decoupling capacitance near the 80960JD, since the processor can cause transient power surges.

Pay special attention to the Test Reset ($\overline{TRST}$) pin. It is necessary to reset the Test Access Port (TAP) controller even if it will not be used. If using the TAP Controller, connect a pulldown resistor between the $\overline{TRST}$ pin and V_{SS}. If the JTAG Boundary Scan function will not be used (even for board-level testing), the $\overline{TRST}$ pin must remain connected to V_{SS}. The resistor, however, may be omitted.

Pins identified as NC must not be connected in the system.

4.4 DC Specifications

Table 13. Targeted 80960JD DC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage	2.4 V_{CC} - 0.5			V	I_{OH} = -1 mA I_{OH} = -200 µA
I_{LI1}	Input Leakage Current for each pin except TCK, TDI, $\overline{TRST}$ and TMS			± 5	µA	$0 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current for TCK, TDI, $\overline{TRST}$ and TMS		-140	-250	µA	V_{IN} = 0.45V (1)
I_{LO}	Output Leakage Current			± 5	µA	$0.4 \le V_{OUT} \le V_{CC}$

NOTES:

1. These pins have internal pullup devices. Typical leakage current is not tested.
2. Measured with device operating and outputs loaded to the test condition in Figure 8, AC Test Load (pg. 27).
3. I_{CC} Minimum is measured at minimum V_{CC} and maximum temperature. This parameter is characterized but not tested.
4. I_{CC} Typical is measured at nominal V_{CC} and T_C = 25 °C. This parameter is characterized but not tested.
5. I_{CC} Maximum is measured at maximum V_{CC} and minimum temperature. This parameter is fully tested.
6. Not tested.

Table 13. Targeted 80960JD DC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_{CC}	Power Supply Current (80960JD-50)					
	I_{CC} Operating	400	525	640	mA	(2,3,4,5)
	I_{CC} Halt mode		51	56		(4,5)
	I_{CC} ONCE mode		19	30		(4,5)
I_{CC}	Power Supply Current (80960JD-40)					
	I_{CC} Operating	330	430	530	mA	(2,3,4,5)
	I_{CC} Halt mode		40	44		(4,5)
	I_{CC} ONCE mode		19	30		(4,5)
I_{CC}	Power Supply Current (80960JD-33)					
	I_{CC} Operating	275	365	450	mA	(2,3,4,5)
	I_{CC} Halt mode		33	36		(4,5)
	I_{CC} ONCE mode		19	30		(4,5)
C_{IN}	Input Capacitance					$f_{CLKIN} = f_{MIN}$ (6)
	PGA			12	pF	
	PQFP			10		
C_{OUT}	I/O or Output Capacitance					$f_{CLKIN} = f_{MIN}$ (6)
	PGA			12	pF	
	PQFP			10		
C_{CLK}	CLKIN Capacitance					$f_{CLKIN} = f_{MIN}$ (6)
	PGA			12	pF	
	PQFP			10		

NOTES:

1. These pins have internal pullup devices. Typical leakage current is not tested.
2. Measured with device operating and outputs loaded to the test condition in Figure 8, AC Test Load (pg. 27).
3. I_{CC} Minimum is measured at minimum V_{CC} and maximum temperature. This parameter is characterized but not tested.
4. I_{CC} Typical is measured at nominal V_{CC} and T_C = 25 °C. This parameter is characterized but not tested.
5. I_{CC} Maximum is measured at maximum V_{CC} and minimum temperature. This parameter is fully tested.
6. Not tested.

4.5 AC Specifications

Targeted 80960JD AC timings are based upon design simulation at 50 MHz. Revised information for all frequency grades will be published upon the completion of device characterization. Contact your local Intel representative before finalizing a design.

Table 14. Targeted 80960JD Input Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T_F	CLKIN Frequency	8	25	MHz	
T_C	CLKIN Period	40	125	ns	
T_{CS}	CLKIN Period Stability		±0.1	%Δ	Adjacent Clocks (1)
T_{CH}	CLKIN High Time	16		ns	Measured at 1.5 V (1)
T_{CL}	CLKIN Low Time	16		ns	Measured at 1.5 V (1)
T_{CR}	CLKIN Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{CF}	CLKIN Fall Time		5	ns	2.0 V to 0.8 V (1)

NOTES:
1. Not tested.

Table 15. Targeted 80960JD Synchronous Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{OV1}	Output Valid Delay, Except ALE/$\overline{ALE}$ Inactive and DT/$\overline{R}$	3	17	ns	
T_{OV2}	Output Valid Delay, DT/$\overline{R}$	0.45 T_C + 3	0.55 T_C + 17	ns	
T_{OF}	Output Float Delay	3	17	ns	(1)

NOTES:
1. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested.

Table 16. Targeted 80960JD Synchronous Input Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{IS1}	Input Setup to CLKIN — AD31:0, $\overline{NMI}$, $\overline{XINT7:0}$	8		ns	(1)
T_{IH1}	Input Hold from CLKIN — AD31:0, $\overline{NMI}$, $\overline{XINT7:0}$	2		ns	(1)
T_{IS2}	Input Setup to CLKIN — $\overline{RDYRCV}$ and HOLD	10		ns	(2)
T_{IH2}	Input Hold from CLKIN — $\overline{RDYRCV}$ and HOLD	1		ns	(2)
T_{IS3}	Input Setup to CLKIN — $\overline{RESET}$	8		ns	(3)
T_{IH3}	Input Hold from CLKIN — $\overline{RESET}$	2		ns	(3)
T_{IS4}	Input Setup to $\overline{RESET}$ — $\overline{ONCE}$, STEST	8		ns	(4)
T_{IH4}	Input Hold from $\overline{RESET}$ — $\overline{ONCE}$, STEST	2		ns	(4)

NOTES:

1. AD31:0 are synchronous inputs. Setup and hold times must be met for proper processor operation. $\overline{NMI}$ and $\overline{XINT7:0}$ may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, $\overline{NMI}$ and $\overline{XINT7:0}$ must be asserted for a minimum of two CLKIN periods to guarantee recognition.
2. $\overline{RDYRCV}$ and HOLD are synchronous inputs. Setup and hold times must be met for proper processor operation.
3. $\overline{RESET}$ may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
4. $\overline{ONCE}$ and $\overline{STEST}$ must be stable at the rising edge of $\overline{RESET}$ for proper operation.

Table 17. Targeted 80960JD Relative Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{LXL}	ALE/$\overline{ALE}$ Width	$0.45T_C$ -3		ns	(1)
T_{LXA}	Address Hold from ALE/$\overline{ALE}$ Inactive	$0.45T_C$ -3		ns	Equal Loading (1)
T_{DXD}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Active	$0.45T_C$ -3		ns	Equal Loading (1)

NOTES:

1. Guaranteed by design. May not be 100% tested.

Table 18. Targeted 80960JD Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency		8	MHz	
T_{BSC}	TCK Period	125		ns	
T_{BSCH}	TCK High Time	40		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	40		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		8	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		8	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	8		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	10		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	Relative to falling edge of TCK
T_{BSOF1}	TDO Float Delay	3	36	ns	Relative to falling edge of TCK
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to falling edge of TCK
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	36	ns	Relative to falling edge of TCK
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	8		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	10		ns	

NOTES:
1. Not tested.

4.5.1 AC Test Conditions and Derating Curves

The AC Specifications in **Section 4.5, AC Specifications** are tested with the 50 pF load indicated in Figure 8. Figure 9 shows how timings vary with load capacitance; Figure 10 shows how output rise and fall times vary with load capacitance.

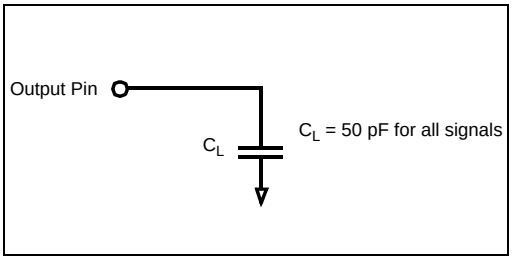


Figure 8. AC Test Load

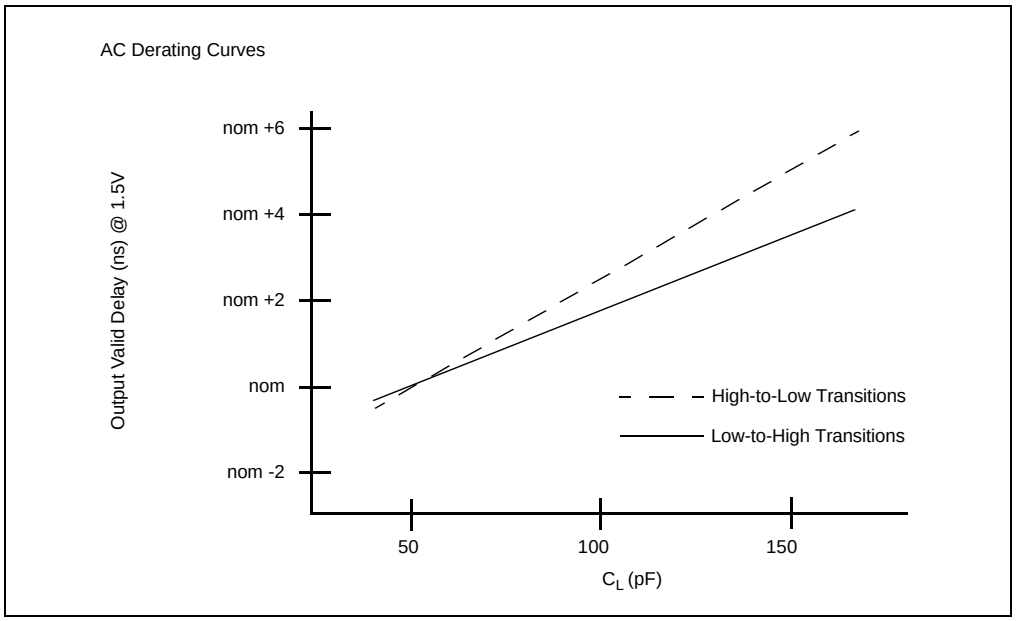


Figure 9. Output Delay or Hold vs. Load Capacitance

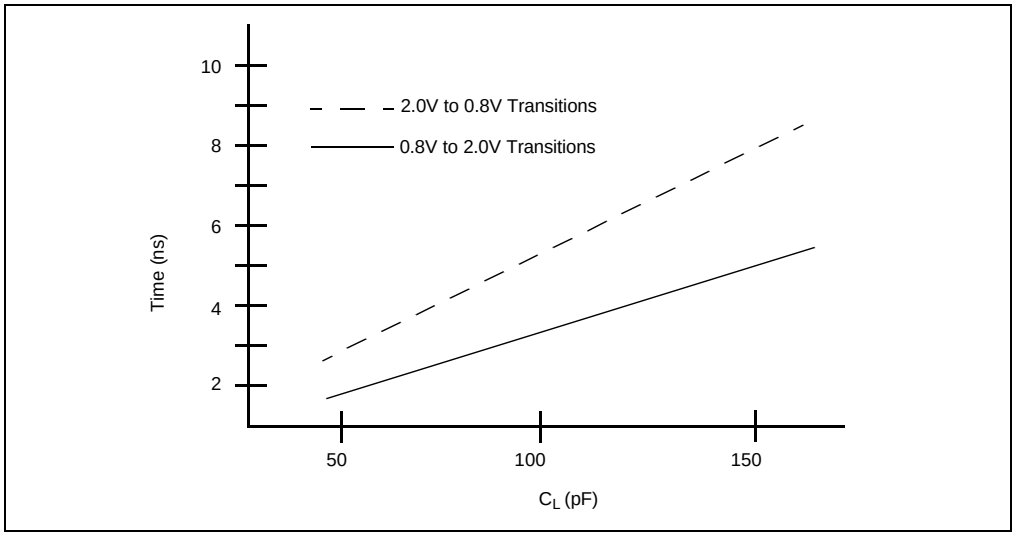


Figure 10. Rise and Fall Time Derating

4.5.2 AC Timing Waveforms

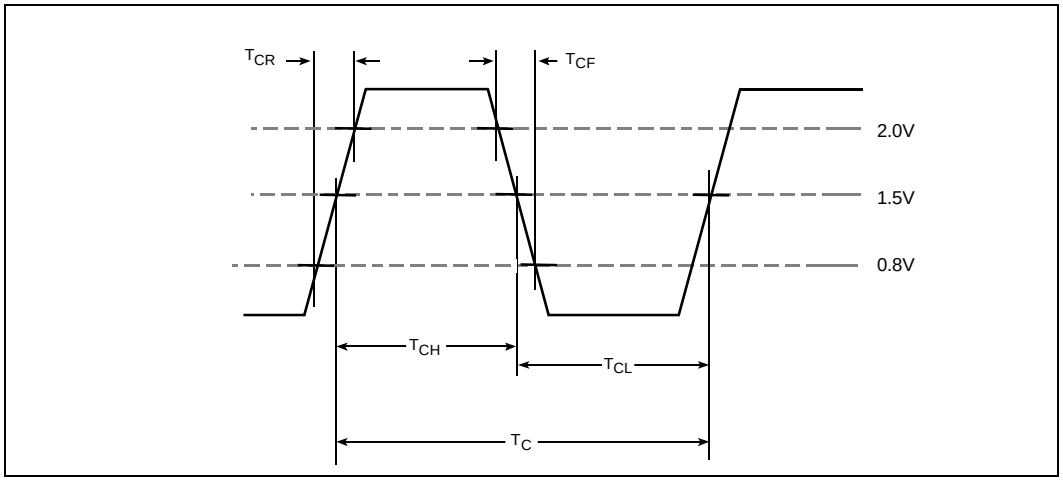


Figure 11. CLKIN Waveform

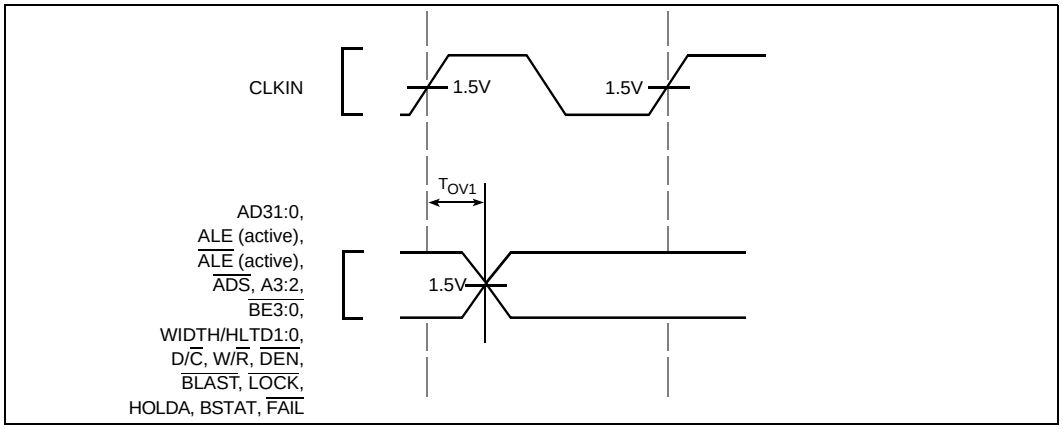


Figure 12. Output Delay Waveform for T_{OV1}

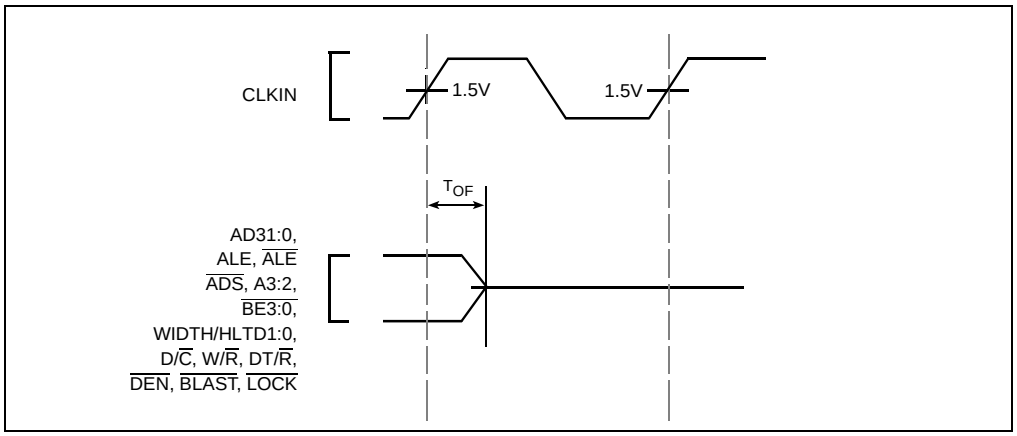


Figure 13. Output Float Waveform for T_{OF}

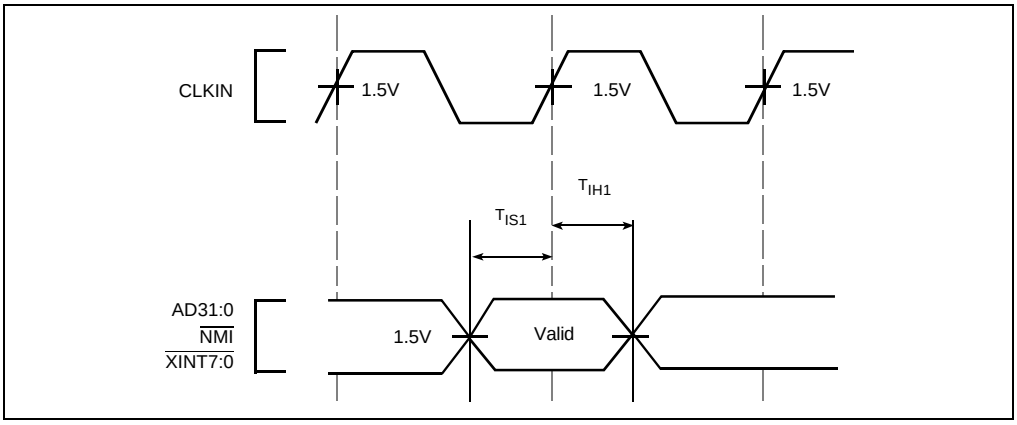


Figure 14. Input Setup and Hold Waveform for T_{IS1} and T_{IH1}

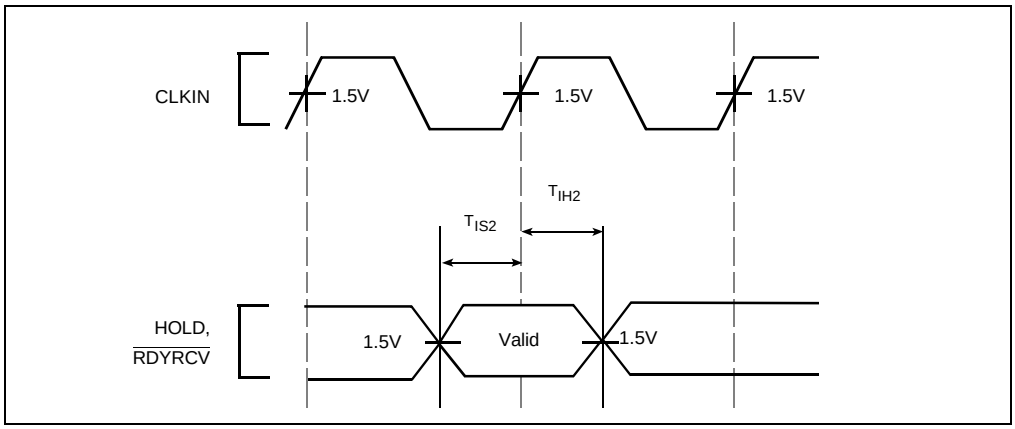


Figure 15. Input Setup and Hold Waveform for T_{IS2} and T_{IH2}

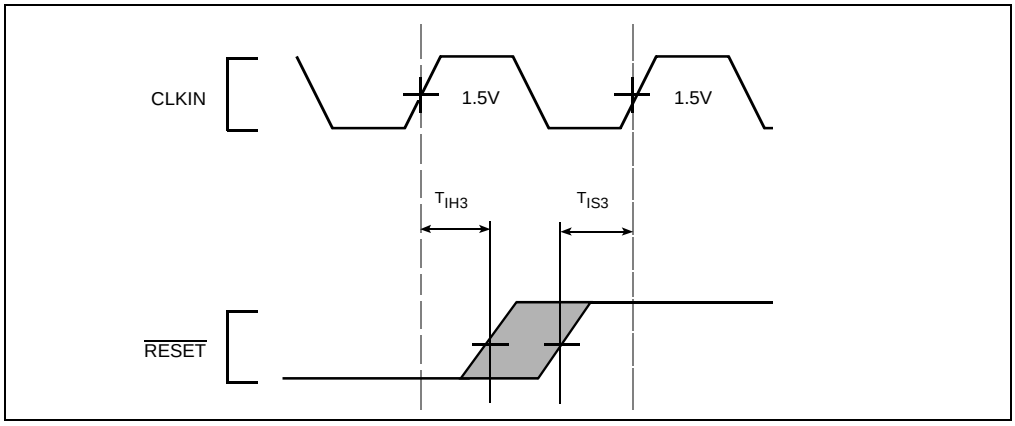


Figure 16. Input Setup and Hold Waveform for T_{IS3} and T_{IH3}

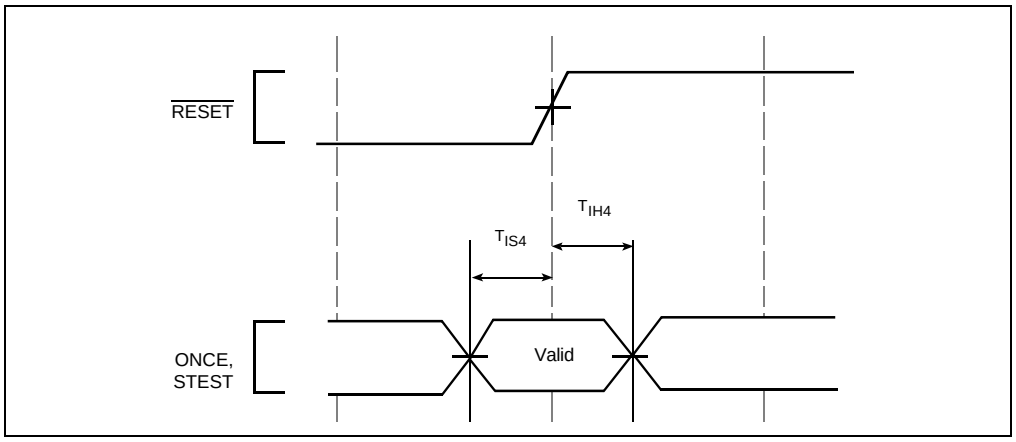


Figure 17. Input Setup and Hold Waveform for T_{IS4} and T_{IH4}

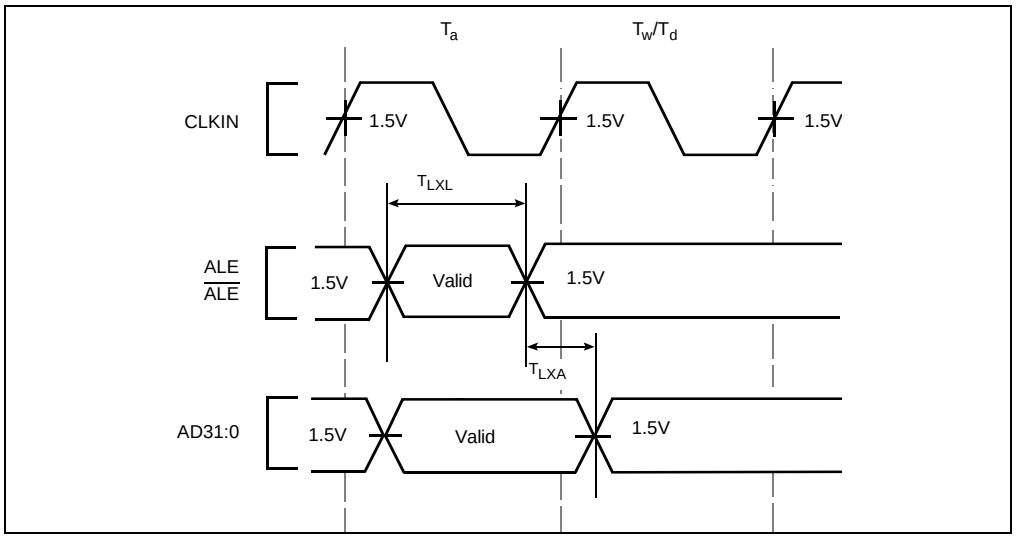


Figure 18. Relative Timings Waveform for T_{LXL} and T_{LXA}

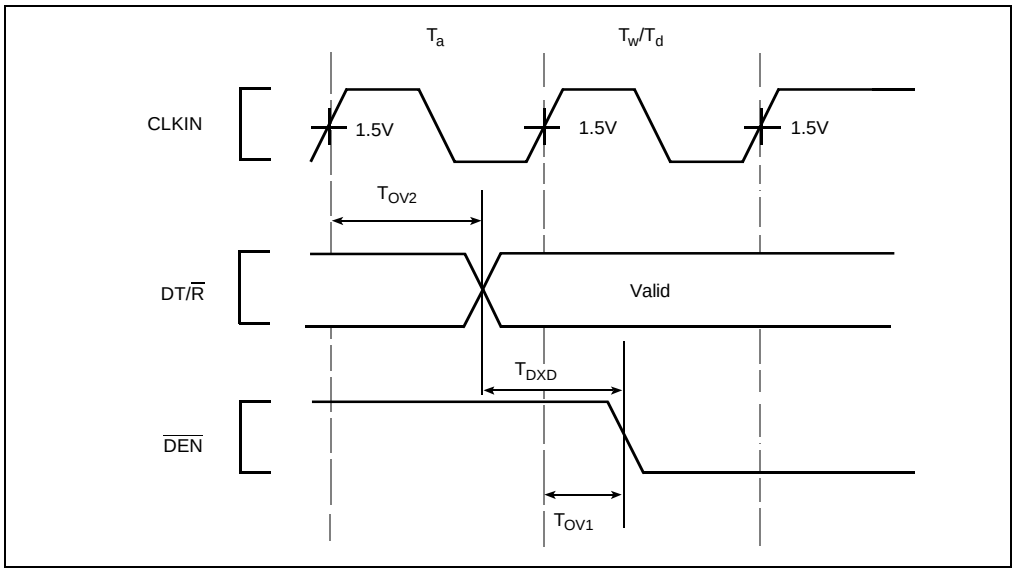


Figure 19. DT/$\overline{R}$ and $\overline{DEN}$ Timings Waveform

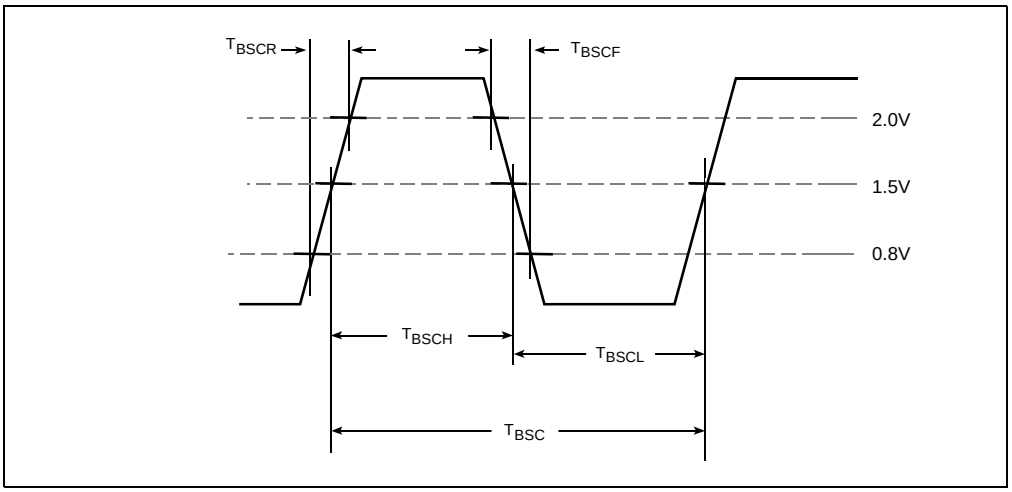


Figure 20. TCK Waveform

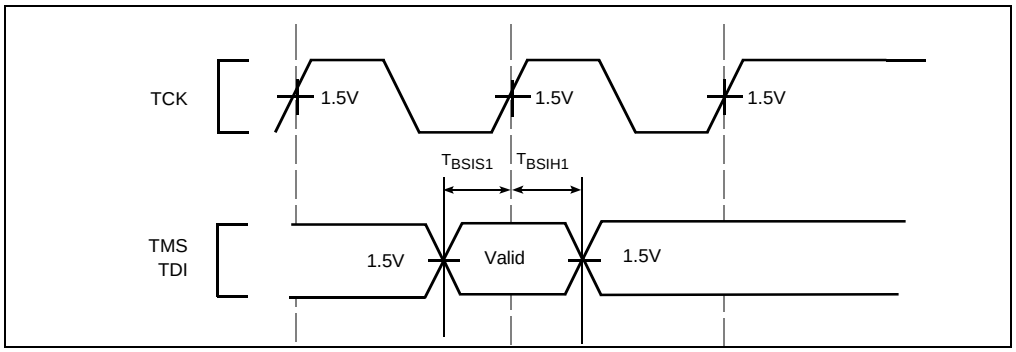


Figure 21. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}

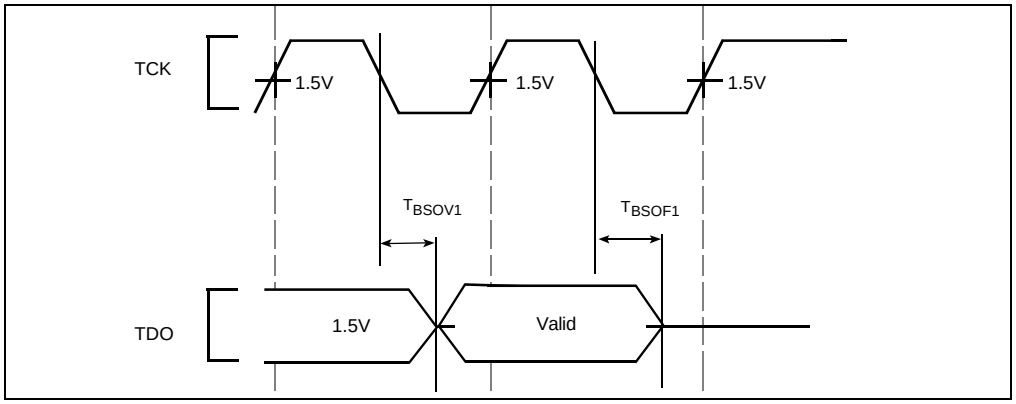


Figure 22. Output Delay and Output Float for T_{BSOV1} AND T_{BSOF1}

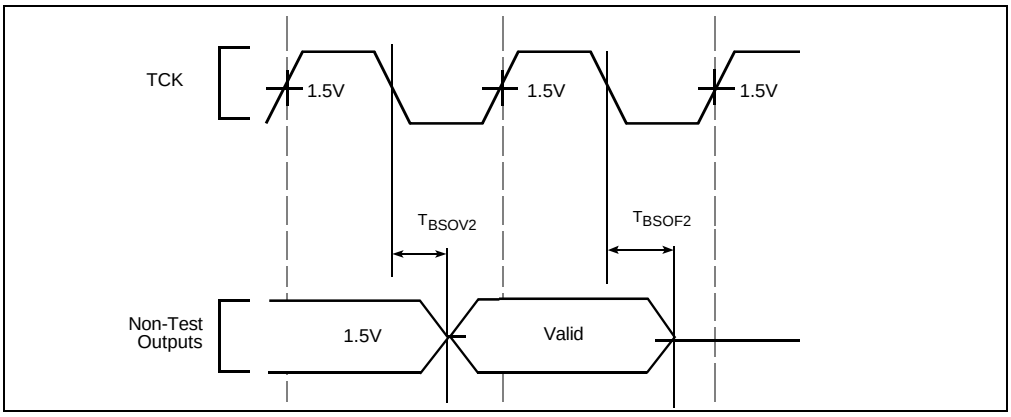


Figure 23. Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2}

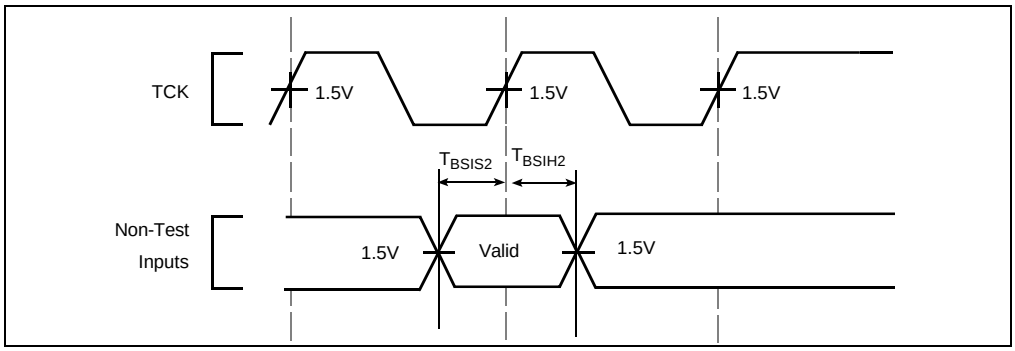


Figure 24. Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2}

5.0 BUS FUNCTIONAL WAVEFORMS

Figures 25 through 30 illustrate typical 80960JD bus transactions. Figure 31 depicts the bus arbitration sequence. Tables 19 through 22 summarize all possible combinations of bus accesses across 8-, 16-, and 32-bit buses according to data alignment. Figures 32 and 33 also show accesses on 32-bit buses. Figure 34 illustrates the processor reset sequence from the time power is applied to the device.

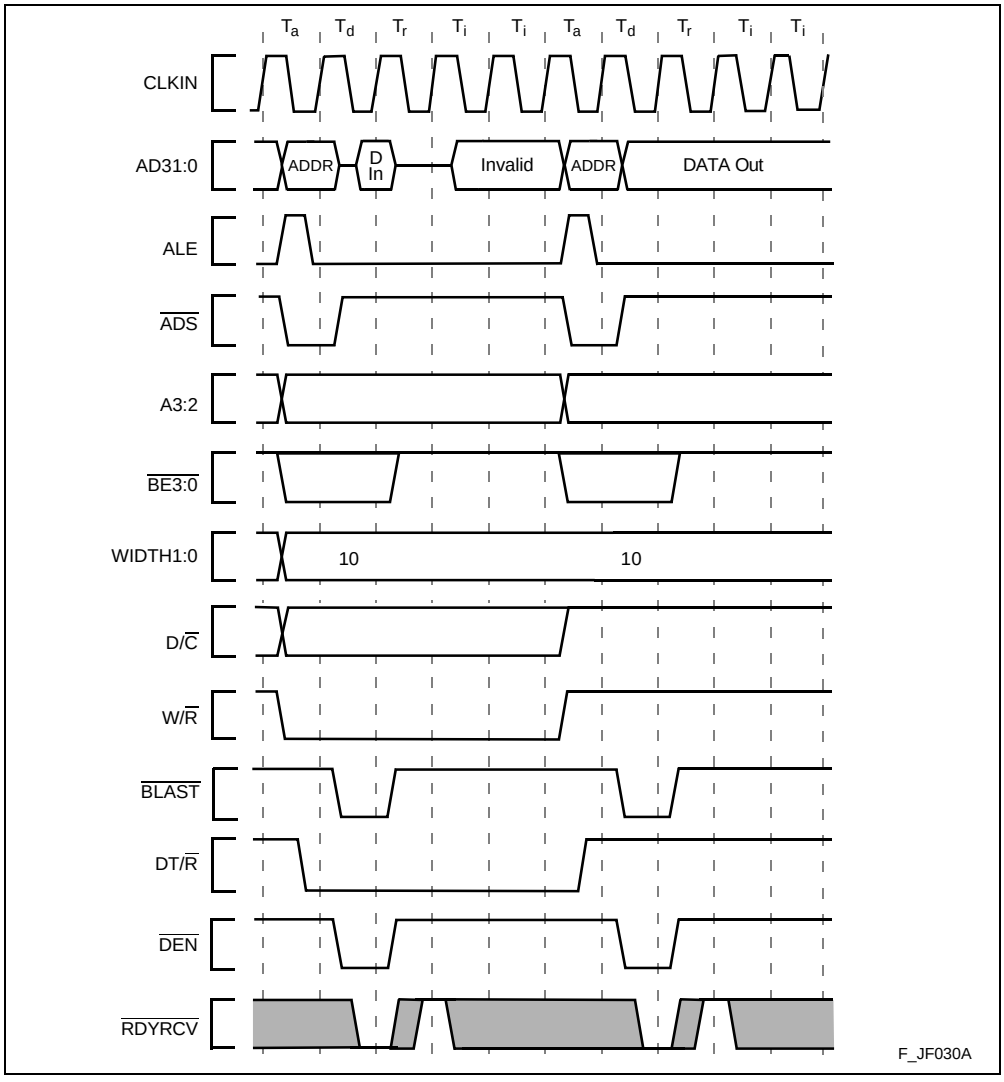


Figure 25. Non-Burst Read and Write Transactions Without Wait States, 32-Bit Bus

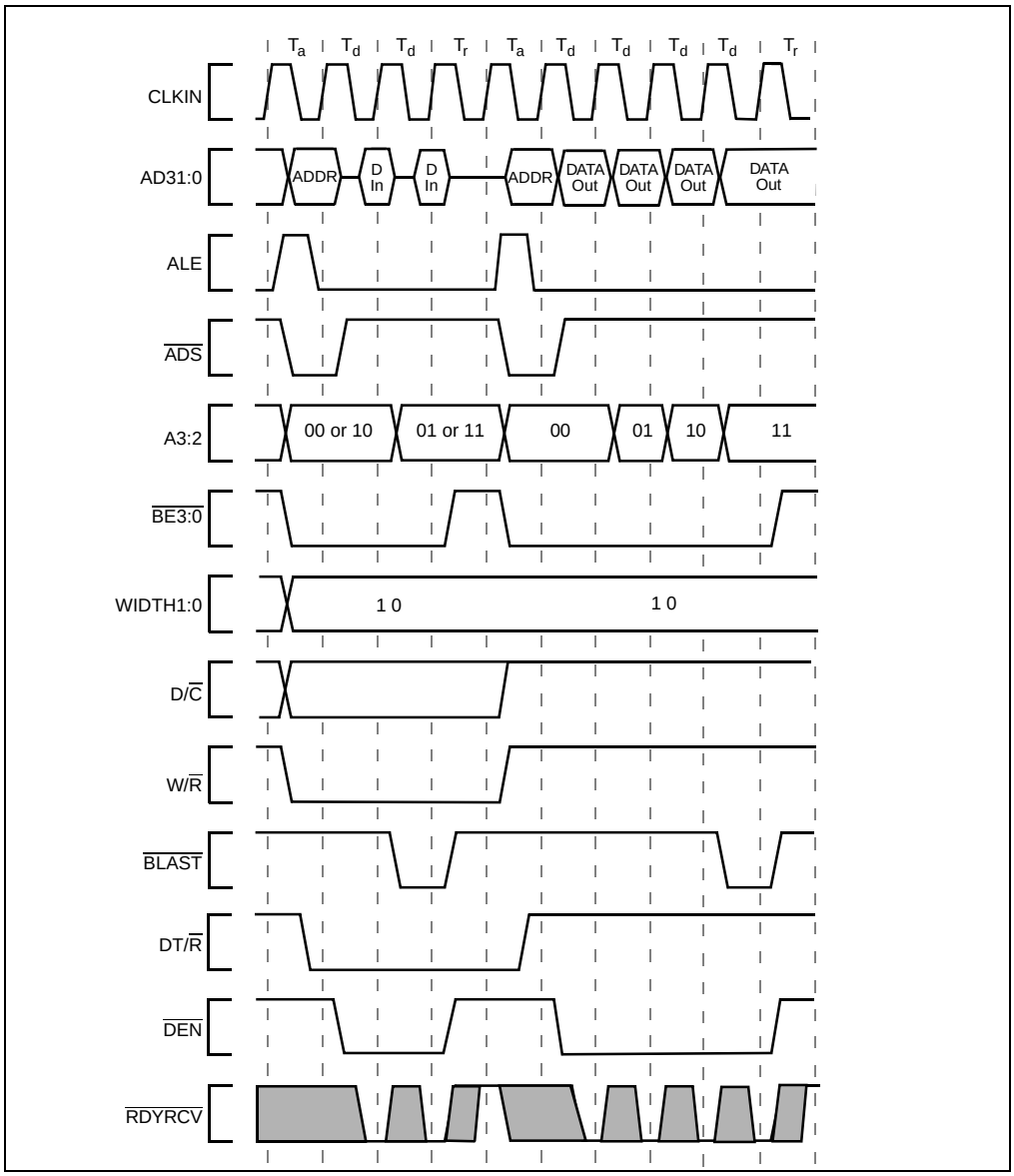


Figure 26. Burst Read and Write Transactions Without Wait States, 32-Bit Bus

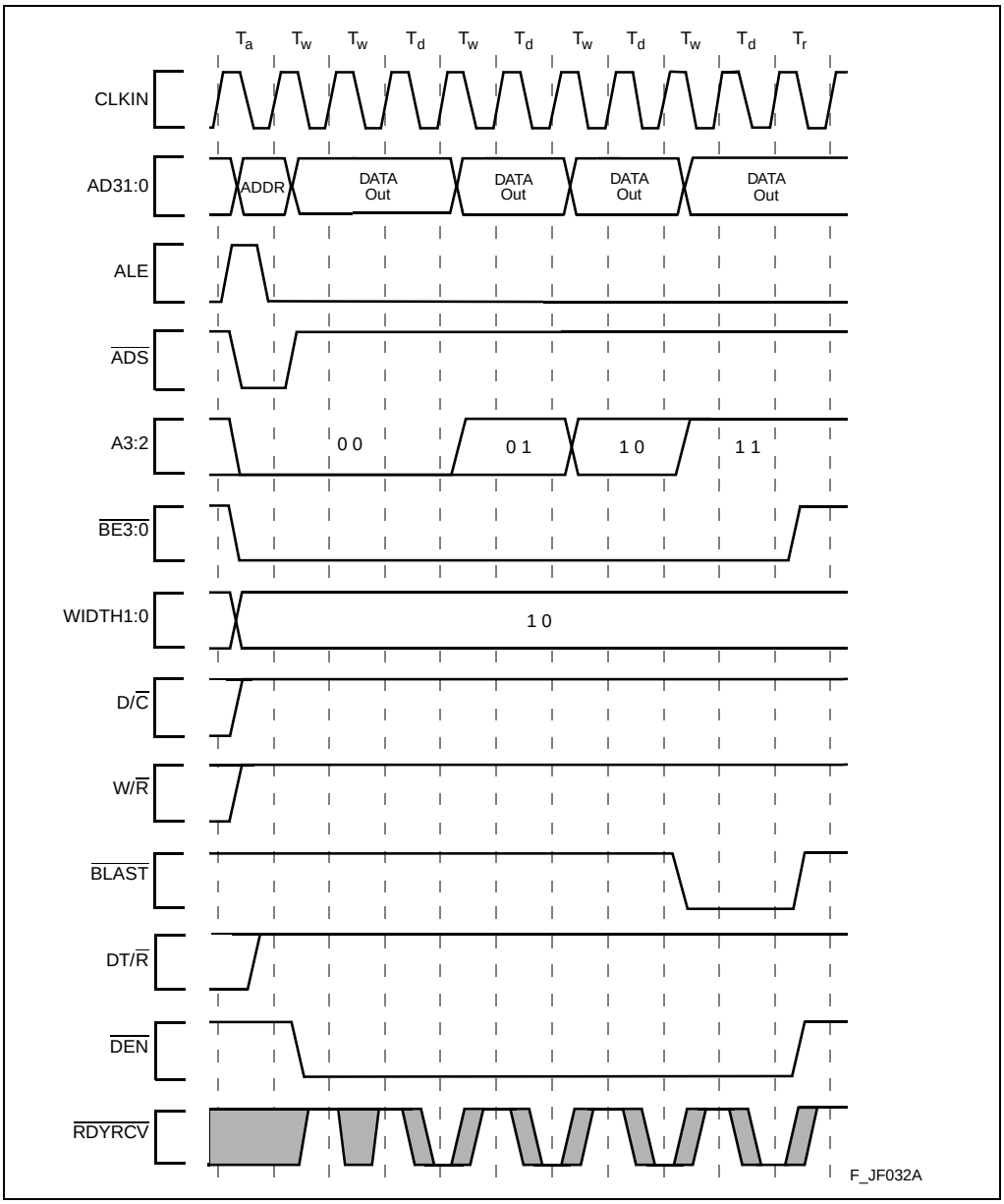


Figure 27. Burst Write Transactions With 2,1,1,1 Wait States, 32-Bit Bus

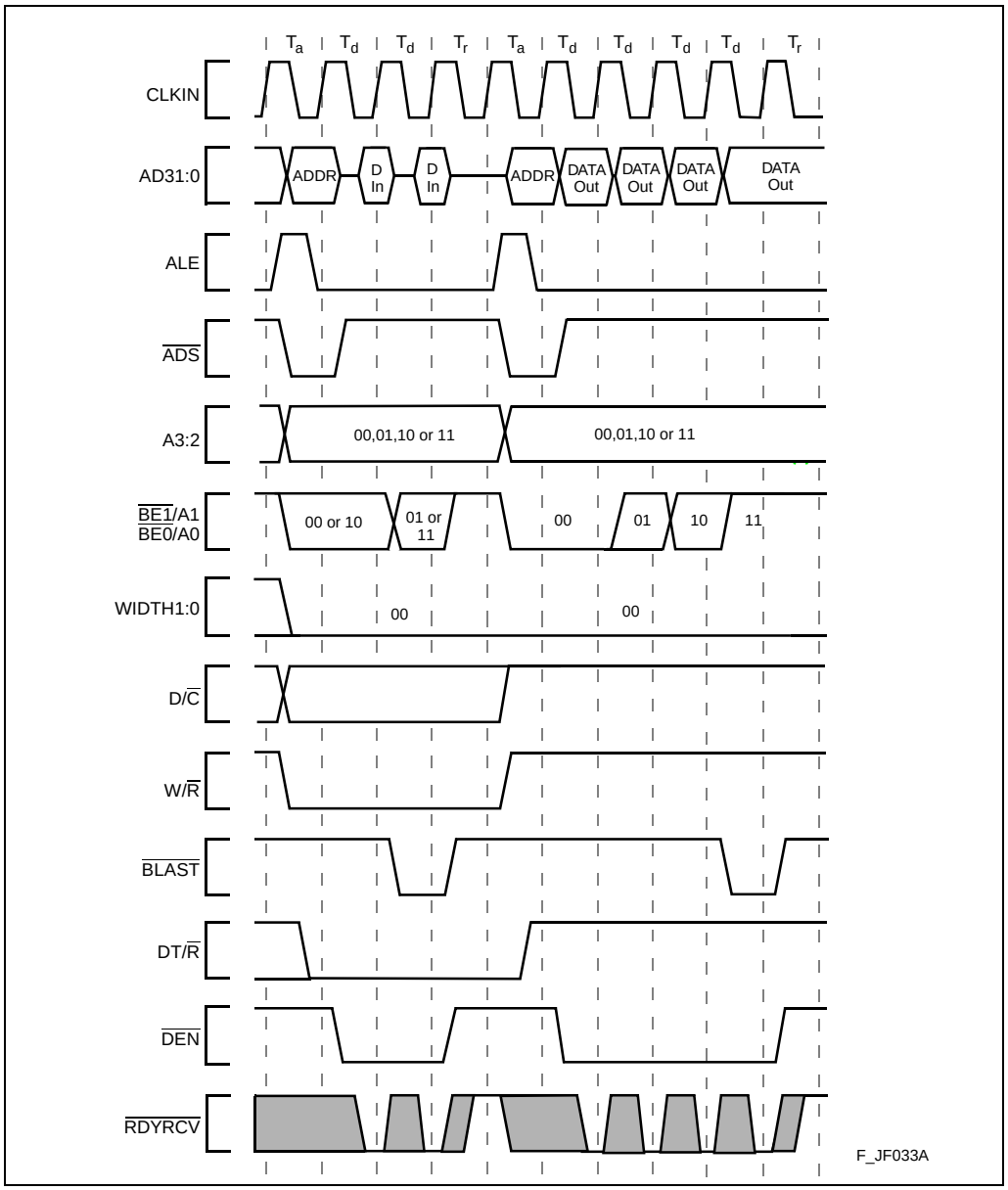


Figure 28. Burst Read and Write Transactions Without Wait States, 8-Bit Bus

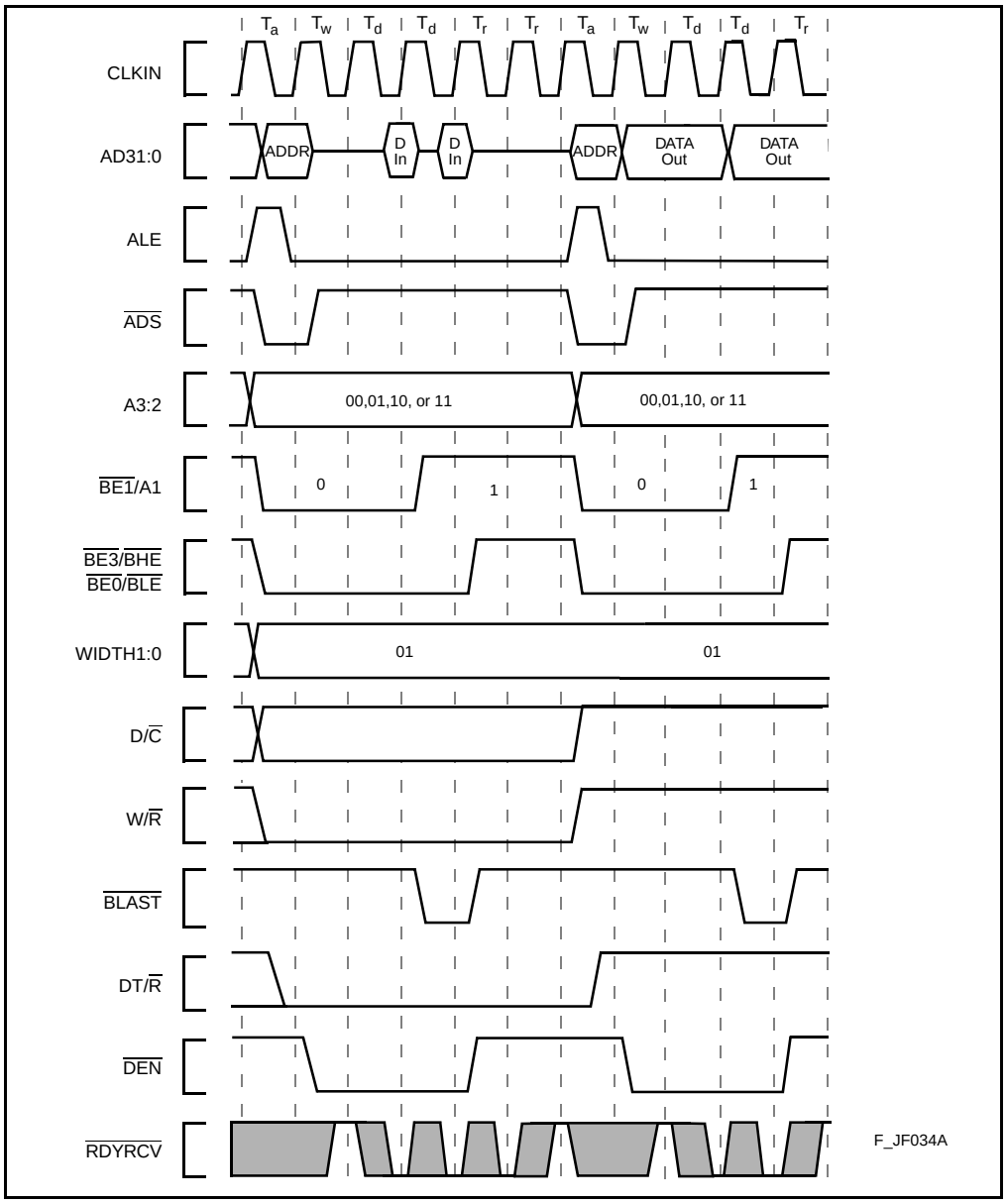


Figure 29. Burst Read and Write Transactions With 1, 0 Wait States and Extra Tr State on Read, 16-Bit Bus

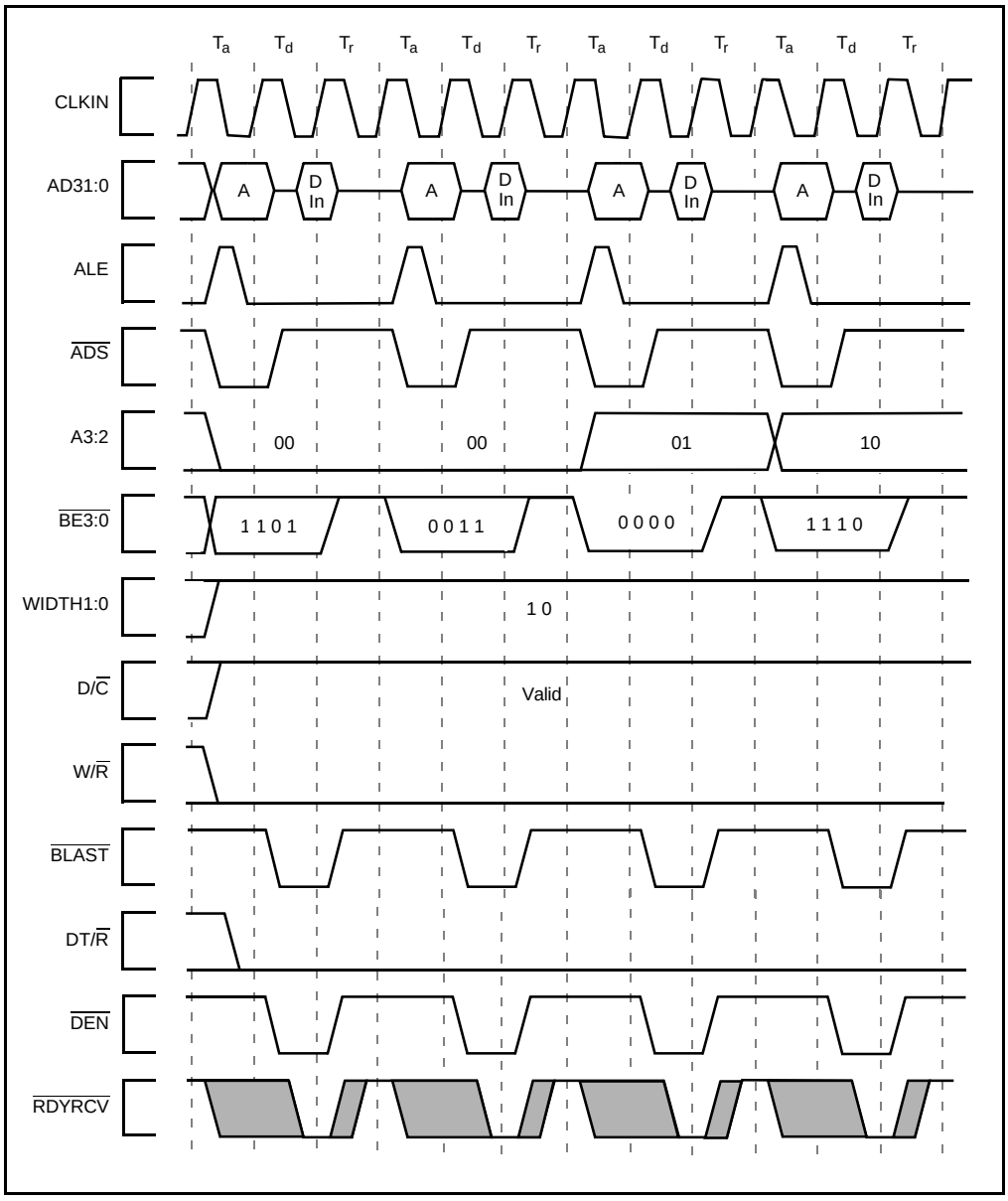
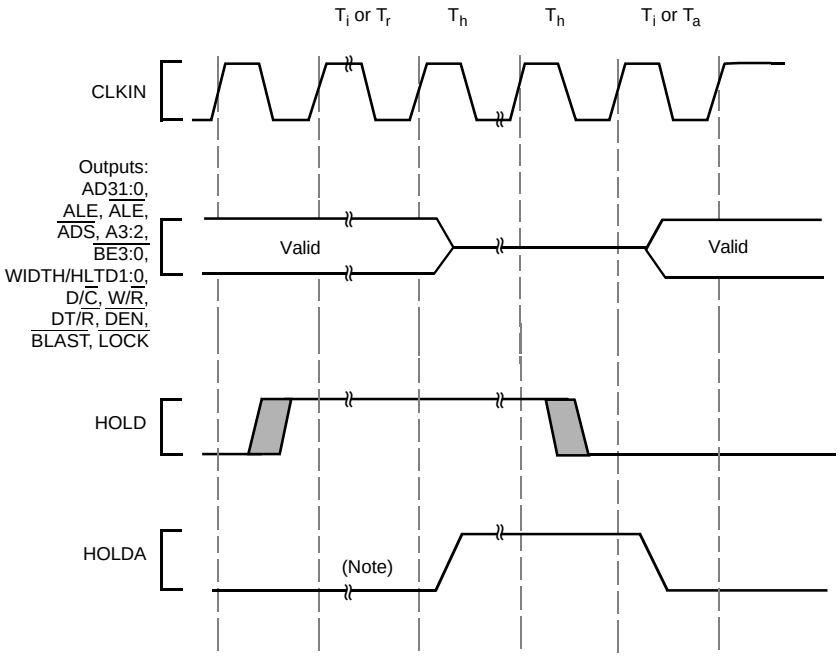


Figure 30. Bus Transactions Generated by Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit Bus, Little Endian



NOTE: HOLD is sampled on the rising edge of CLKIN. The processor asserts HOLDA to grant the bus on the same edge in which it recognizes HOLD if the last state was T_i or the last T_r of a bus transaction. Similarly, the processor deasserts HOLDA on the same edge in which it recognizes the deassertion of HOLD.

Figure 31. HOLD/HOLDA Waveform For Bus Arbitration

Table 19. Natural Boundaries for Load and Store Accesses

Data Width	Natural Boundary (Bytes)
Byte	1
Short Word	2
Word	4
Double Word	8
Triple Word	16
Quad Word	16

Table 20. Summary of Byte Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	• byte access	• byte access	• byte access

Table 21. Summary of Short Word Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	• burst of 2 bytes	• short-word access	• short-word access
+1	• 2 byte accesses	• 2 byte accesses	• 2 byte accesses

Table 22. Summary of *n*-Word Load and Store Accesses (*n* = 1, 2, 3, 4)

Address Offset from Natural Boundary in Bytes	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned) (*n* =1, 2, 3, 4)	• *n* burst(s) of 4 bytes	• case *n*=1: burst of 2 short words • case *n*=2: burst of 4 short words • case *n*=3: burst of 4 short words burst of 2 short words • case *n*=4: 2 bursts of 4 short words	• burst of *n* word(s)
+1 (*n* =1, 2, 3, 4) +5 (*n* = 2, 3, 4) +9 (*n* = 3, 4) +13 (*n* = 3, 4)	• byte access • burst of 2 bytes • *n*-1 burst(s) of 4 bytes • byte access	• byte access • short-word access • *n*-1 burst(s) of 2 short words • byte access	• byte access • short-word access • *n*-1 word access(es) • byte access
+2 (*n* =1, 2, 3, 4) +6 (*n* = 2, 3, 4) +10 (*n* = 3, 4) +14 (*n* = 3, 4)	• burst of 2 bytes • *n*-1 burst(s) of 4 bytes • burst of 2 bytes	• short-word access • *n*-1 burst(s) of 2 short words • short-word access	• short-word access • *n*-1 word access(es) • short-word access
+3 (*n* =1, 2, 3, 4) +7 (*n* = 2, 3, 4) +11 (*n* = 3, 4) +15 (*n* = 3, 4)	• byte access • *n*-1 burst(s) of 4 bytes • burst of 2 bytes • byte access	• byte access • *n*-1 burst(s) of 2 short words • short-word access • byte access	• byte access • *n*-1 word access(es) • short-word access • byte access
+4 (*n* = 2, 3, 4) +8 (*n* = 3, 4) +12 (*n* = 3, 4)	• *n* burst(s) of 4 bytes	• *n* burst(s) of 2 short words	• *n* word access(es)

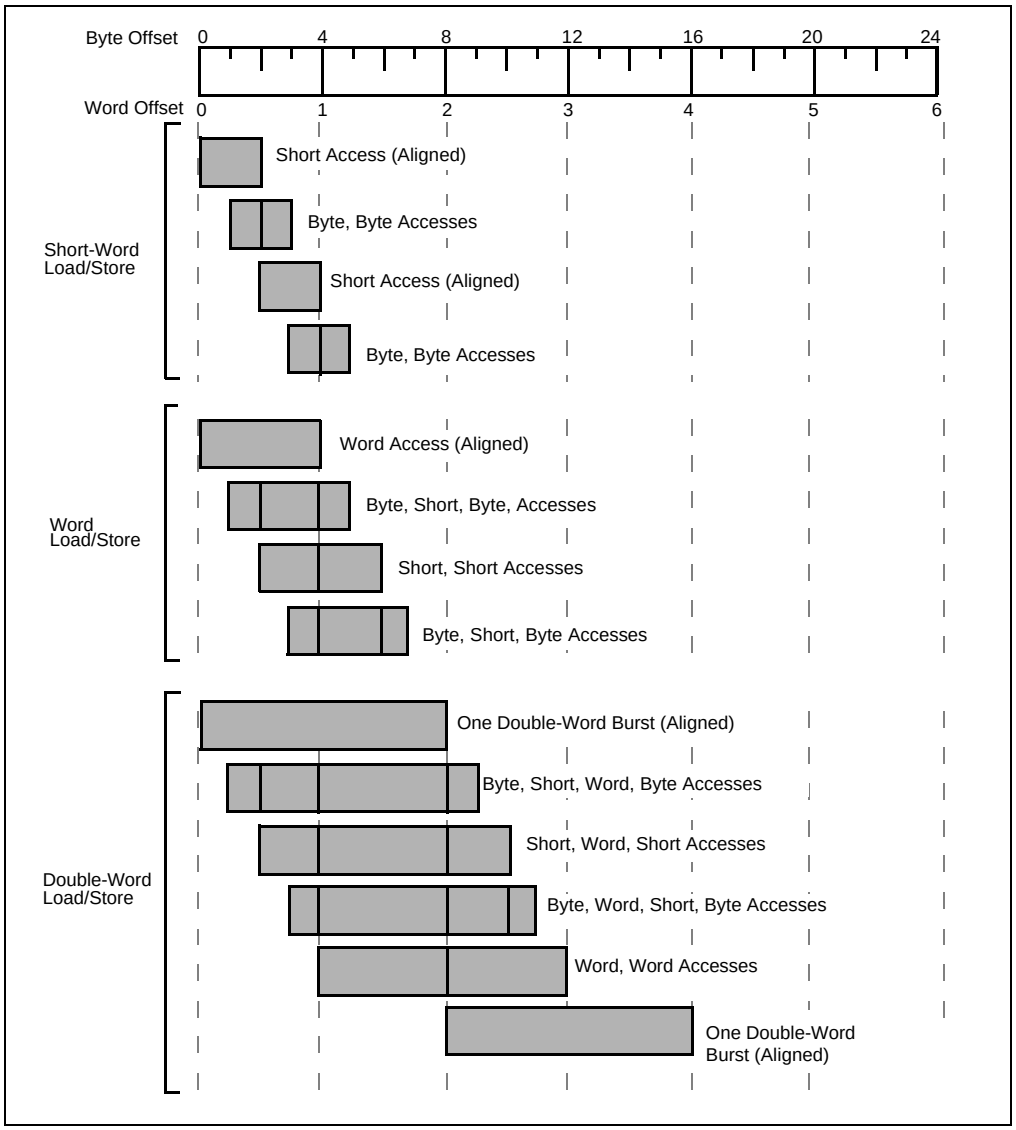


Figure 32. Summary of Aligned and Unaligned Accesses (32-Bit Bus)

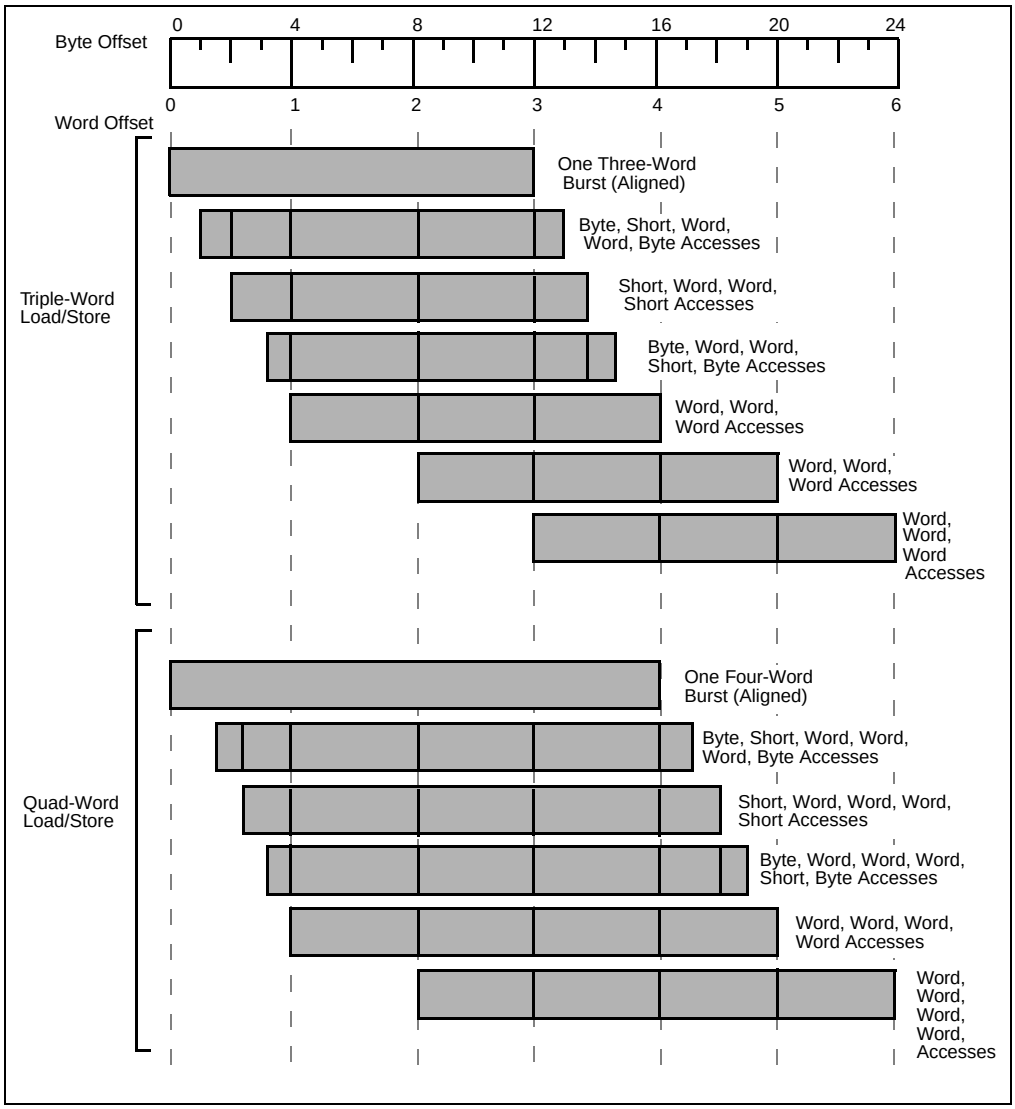


Figure 33. Summary of Aligned and Unaligned Accesses (32-Bit Bus) (Continued)

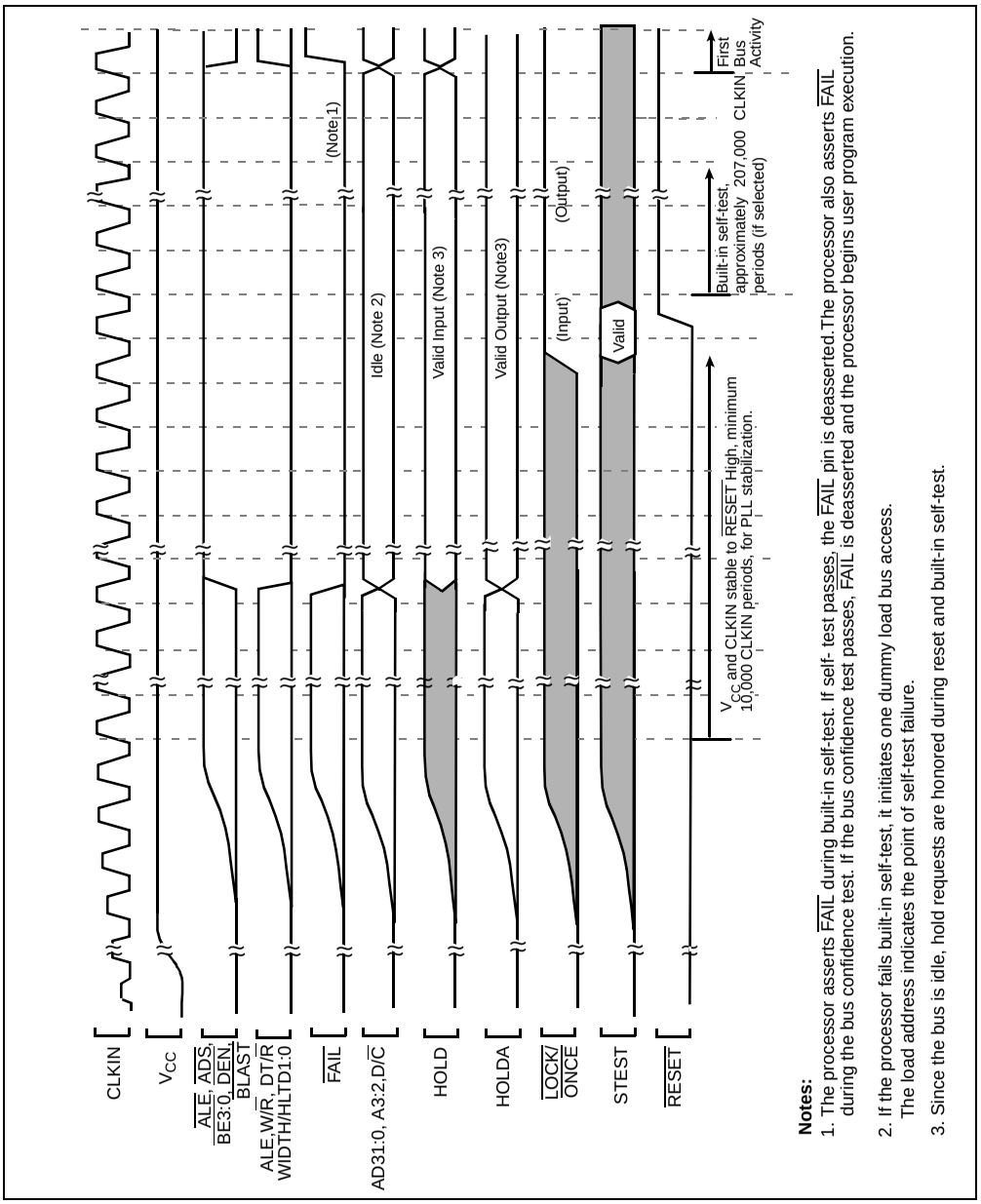


Figure 34. Cold Reset Waveform

6.0 DEVICE IDENTIFICATION

80960JD processors may be identified electrically according to device type and stepping (see Table 23). The 32-bit identifier is accessible in three ways:

- Upon reset, the identifier is placed into the g0 register.
- The identifier may be accessed from supervisor mode at any time by reading the DEVICEID register at address FF008710H.
- The IEEE Standard 1149.1 Test Access Port may select the DEVICE ID register through the IDCODE instruction.

The stepping number is also printed on the top side of the product package.

Table 23. 80960JD Die and Stepping Reference

Device and Stepping	Version Number	Part Number	Manufacturer	X	Complete ID (Hex)
80960JD A0, A2	0000	1000 1000 0010 0000	0000 0001 001	1	08820013